EVOLUTIONARY DESIGN OF DIGITAL CIRCUITS AT TRANSISTOR LEVEL

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Abstract: This work aims to achieve automated design process of integrated circuits on the transistor level using evolutionary algorithm. For this purpose it is necessery to choose suitable level of abstraction during simulation. Proper level of simulation is needed for evaluating candidate circuit solutions by fitness function. This simulation has to be fast enough to evaluate thousands of candidate solutions within seconds. This work discusses already used simulation techniques and it chooses usefull parts for creating faster and effective digital circuit evaluation.

Keywords: evolutionary algorithm, logical circuit design, transistor level, CMOS technology, logical circuit simulation

1 INTRODUCTION

Design of digital circuits can be done by conventional methods on a gate-level. This approach can work well only until certain level of complexity is reached. Then hierarchical design must be applied. By conventional hierarchical design, transistor level circuit representation is created by replacing each gate by its transistor circuit representation, provided by technological design library. This needs to be done even in the case of evolutionary design at the gate-level.

1.1 MOTIVATION

In the case of transistor-level evolutionary design, it was discovered that, more optimized circuit designs can be achieved[1]. This is possible because certain parts of circuit can be efficiently shared in unconventional way and also because smaller building blocks (transistors) allow us to wire more circuits than commonly used gates(NAND, NOR, XOR). When a design or optimization of certain circuit on transistor level is started, there are usually some constraints, which are to be met. Let's call them criteria of optimization. These criteria can be quite simple, such as minimal transistor count, or high reliability, variability tolerance and etc.. On the other hand they can be also multi-objective, where fitness of proposed transistor circuit should meet several requirements at the same time.
Let's list the important criteria:

minimal transistor count,
minimal area usage,
full output voltage swing,
low dynamic and static power consumption,
high maximal operation frequency,
minimal delay in critical path,
hazard free solution.

But these possibly more optimized circuits need to be evaluated with corresponding fitness function. And here come certain limitations of this approach. Evaluation of circuit at the transistor level is more complicated, than gate-level evaluation.

We have studied several approaches to circuit simulation:

- idealistic switch level simulation
- event-based simulation using special circuit simulator proposed in [2]
- analog circuit simulation using SPICE [3]

Idealistic switch level simulation is very fast, but due imperfect conductivity of open transistors, voltage V_t loss problem causes that circuits which work in the simulation, does not work in real implementation.

Event-based simulation, which takes into consideration imperfection of transistor switch-like conductivity, suffer from signal loop propagation, which is problematically detected.

SPICE based simulation is very realistic but also very slow for the purpose of fitness evaluation.

Since any of these approaches have not been very effective in evolving more complex circuits than binary adders we have come up with different approach based on "analytic"(path-finding) solution of circuit signal propagation.

1.2 CARTESIAN GENETIC PROGRAMMING

For automated design process based on evolutionary algorithm, we need to use proper representation of circuit. We chose to use Cartesian genetic programming[1] which is also usually used for gate-level circuit design. Current system is based on chromosome representation, where transistors interconnect circuit nodes. Number of common nodes can be specified to speed-up solution search at right complexity level. Except common nodes, there are also specific nodes, which have to be always present: Vcc, Gnd, $IN_0, \ldots, OUT_n$. More details about CGP can be found in [1].

2 CIRCUIT SIGNAL PATH-FINDING SIMULATION

We propose following simulation method based on graph circuit representation. Transistor can be seen as interconnection of two segments, where one segment of circuit(graph) is connected to the drain and other is connected to the source electrode. Segments are connected when the transistor is open (i.e. positive voltage is applied to the gate electrode) and disconnected when transistor is closed.

If circuit does not contain any problematic loops and it is electronically correct, (practically all conventional designs of logical circuits are, but evolutionary created ones don't have to be) we start to identify all possible paths from output into any signal source.
Signal source can be: Vcc, Gnd, primary (circuit) input.

2.1 ELECTRONIC VALIDITY

We should try to evaluate if circuit is valid from electronic point of view, for this moment ignoring input vectors and reference output. We need to find out if there is possible shortcut inside the circuit. To do that, we will search for: path from *Vcc to Gnd*, path from any *primary input to Vcc* and path from any *primary input to Gnd*.

The simulator searches for all possible signal paths using Breadth First Search algorithm in combination with limited maximal depth of a path. When such path is found all transistors which are on this way should be putted into list coupled with this path. For each transistor we need to evaluate his condition, if it is opened or not. That can be done only by tracing connection from the transistor gate to all possible signal sources.

At the end when all transistor gate paths are found, and there is no cycle (for example all transistor gates are connected directly to the primary inputs of the circuit, as is shown on following scheme

Fig.1), we need to check if there is combination of variable states(inputs) which would lead to shortcut. To do that, equations need to be formulated from the circuit path. The serial connection of transistors put their gate variables into logical AND relation and the parallel one into logical OR relation.

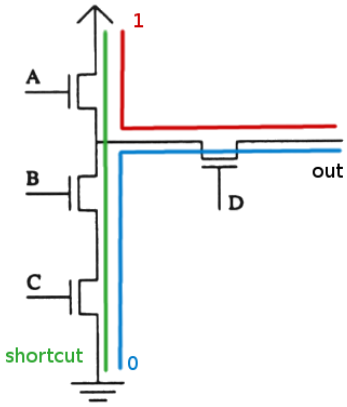

Figure 1: Circuit illustrating signal paths

Equations formulated for showed circuit possible paths would be following:
$shortcut = A.B.C$
$out(1) = A.D.\overline{B.C}$
$out(0) = \overline{A}.D.B.C$

If all combinations of input variables are possible or at least if combination A=1, B=1, C=1 is possible, then this circuit should be disqualified completely (because of a shortcut occurrence) or there should be strong penalty for this candidate solution when evolutionary design process is used.

2.2 Circuit quality evaluation

When shortcut is not possible, output signal path equations are evaluated for each possible input combination. Then results are compared with referential table and for each match, fitness value is increased. Fitness value is also modified by criteria of optimization, e.g. low transistor count will increase the fitness value, but lets say high static power consumption will decrease the fitness.

3 CONCLUSION

In this paper analytical signal-path based simulation method was introduced. Based on this circuit evaluation method, fast and efficient evaluation simulator was implemented. Because fitness evaluation is needed, it is the critical part of whole evolutionary transistor level circuit designing system. This method allows to evolve and evaluate relatively complex circuits exceeding complexity of single bit full adder (10-16 transistors), which was until now reached limit[2]. Circuits evolved using this method respect imperfection of CMOS technology and should work properly in real world.

REFERENCES

[1] Miller Julian F.: Cartesian Genetic Programming, Springer, 2011, ISBN 978-80-200-1729-1

[2] Sekanina L., Žaloudek L., Transistor-Level Evolution of Digital Circuits Using a Special Circuit Simulator. Faculty of Information Technology, Brno University of Technology, 2008

[3] Walker, Hilder, Tyrrel. Evolving Variability-Tolerant CMOS Designs. University of York UK, 2008.