MULTICHANNEL (3G) HD-SDI DIGITAL VIDEO SIGNAL CONVERTER

Stanislav Kučera
Master Degree Programme (2.), FEEC BUT
E-mail: xkucer67@stud.feec.vutbr.cz

Supervised by: Soběslav Valach
E-mail: valach@feec.vutbr.cz

Abstract: In this paper, a design of hardware for a multichannel HD-SDI converter is proposed. This proposed converter mediates between six channels of SD, HD or 3G - SDI digital video signal and the 10-Gigabit Ethernet, whose full-duplex physical interface is terminated with SFP+ module. The device is based on a low-cost FPGA, its SDI inputs consists of a cable equalizer and SDI to 5-bit LVDS deserializer. Deserialized SDI data outputs are therefore connected to FPGA standard I/O pins. The overall design is in compliance with necessary rules of high-speed digital design and is adapted to a medium-quantity production.

Keywords: FPGA, HD-SDI, 10-Gigabit Ethernet, Signal Integrity

1 INTRODUCTION

This paper briefly describes the key aspects of hardware design of the multi-channel SDI video signal converter. The intended purpose of the device is to concentrate six HD-SDI cameras output digital video signal and transmit it over standard 10-Gigabit Ethernet interface. Other interfaces and subsystems are together with other constraints implemented as user's requirements.

2 SMPTE SDI STANDARDS

Serial Digital Interface standards created by The Society of Motion Picture and Television Engineers are predominant standards for uncompressed digital video interfaces in the video production and broadcast studio. Examples of the selected parameters of SDI standards are shown in Table 1 [1].

Table 1: Selected parameters of the main SDI standards [1].

Protocol	SMPTE Standard	Bitrate	Video signal
SD-SDI	259M	270 Mb/s	Equivalent to PAL or NTSC.
HD-SDI	292M	1,485 Gb/s	Up to 1920x1080 pix at 30 Hz.
3G-SDI	424M	2,97 Gb/s	Up to 1920x1080 pix at 60 Hz.

The most common video formats are Y'Cb'Cr' component video, the sampling structure is 4:2:2 with 10 bits per component. The payload - Active Video consists of interleaved luminance (Y) and chrominance (C) samples, Active Video is a part of one line in the SDI data stream.

The SDI signal is carried on a single-ended 75 Ω coaxial cables with BNC connectors, these are identical with transmission lines for former analogue technologies. Maximum reachable cable length for correct transmission is up to 400 m (SD-SDI) or 100 - 200 m (HD-SDI).

3 DESIGN OF ELECTRONICS

Block diagram in the Figure 1 shows the architecture of electronics, where main components and interfaces are mentioned.

A requirement to handle such a high bit-rate of six HD-SDI inputs, translate it into packets and send via Ethernet and integrate several others interfaces clearly leads to application of an FPGA as the main computing element. The configuration bitstream is stored in the Flash memory and loaded to the FPGA via SPI.

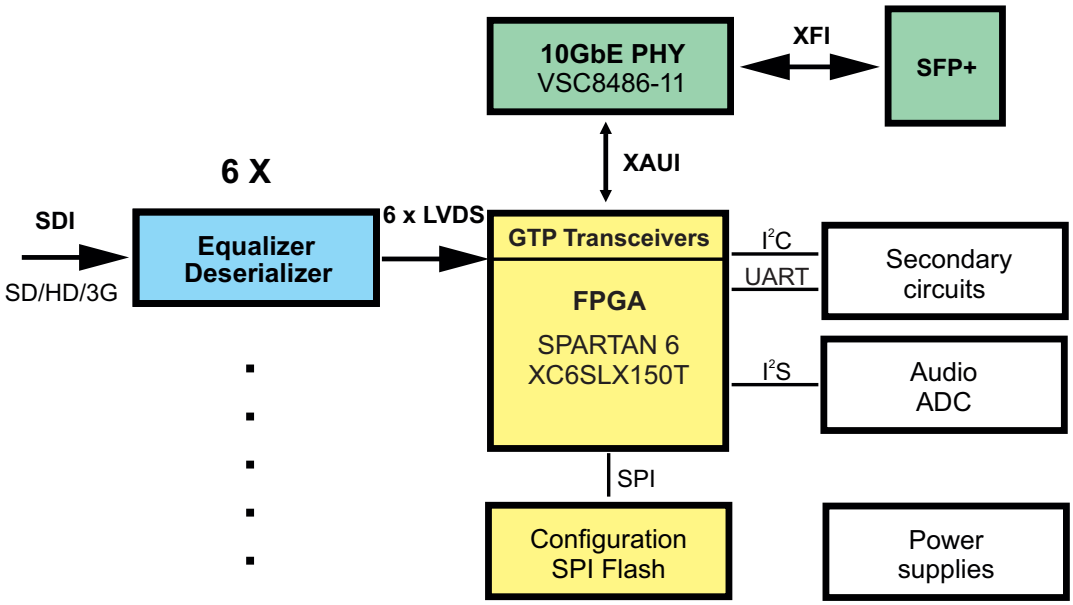

Figure 1: Block diagram of electronics.

This particular FPGA contains four pairs of GTP transceivers utilized for the Ethernet Attachment Unit Interface (XAUI) between 10G-E's Media Access Controller (MAC) and Physical Layer device (PHY). XAUI is extended and more flexible than the initial XGMII (in sum 74 wires), consists of four 8b/10b encoded 3,125 Gb/s data lines for each direction (in sum 8 differential pairs).

The PHY chip converts 4 x 3,125 Gb/s XAUI data to a 10 Gb/s serial stream (XFI) which drives the SFP+ transceiver module for actual physical medium - optical fiber.

The high-quality dual-channel 24-bit ADC provides stereo audio input.

Because components that are used requires multiple power supplies that generate different voltages (e.g. for core, I/O), four switched-mode and four linear regulators are utilized. These regulators are reasonably combined for the maximum overall performance and efficiency.

Converters SDI input channels are described in the following subsection.

3.1 SD/HD/3G SDI INPUT CHANNEL

A typical SDI input channel based on components produced by Texas Instruments is shown in Fig. 2.

The RLC circuit provides impedance matching of single-ended coaxial cable to the differential input of the cable equalizer.

The LMH0344 cable equalizer is based on a multi-stage adaptive filter whose gain and bandwith is set according to the actual signal quality. This equalizer is able to restore the 3G-SDI signal even if its amplitude is only 3 mV (after 180 m of cable at the input), if the SNR has an acceptable value.

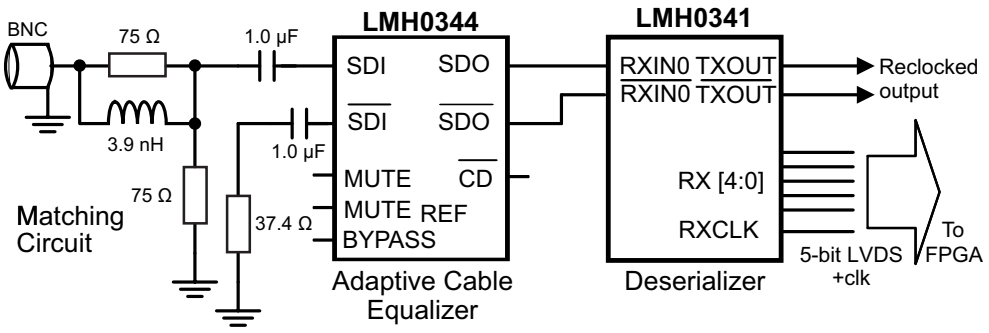

Figure 2: Simplified circuit diagram of one SDI input channel [2].

The LMH0341 deserializer is converting data received by the serial interface to an 5-bit DDR LVDS interface. This allows, in case of compliance with certain rules, connection to FPGA standard input pins.

4 SIGNAL INTEGRITY

Signal integrity is a field of study dealing with the quality of an electrical signal which is being influenced by undesirable effects such as reflections, ringing, crosstalk, dielectric loss, etc.[3]. While the present interfaces reaching 10 Gb/s bitrate, it's necessary to deal with issues named above. The designer should be familiar with techniques like controlled impedance PCB's, their loss (dielectric loss, skin-effect), skew reduction, avoiding impedance discontinuities or stubs, correct termination and interconnection between various logic standards or signal preemphasis and equalization.

5 CONCLUSION

During the design phase of this project, the maximal emphasis has been placed on meeting all the important aspects of high-speed digital systems' design. A thorough analysis of these aspects will be available in the authors master's thesis and will be presented briefly during the defense of this paper. The designed converter was successfully developed and verified under real operating conditions in outdoor environment and is being produced in higher volume. Due to the flexibility of reconfigurable hardware platform, where inputs supports almost all SDI standards, the main device functionality can be matched for various applications. The converter can be a data concentrator in broadcast studio, surveillance system or in CCTV, or even can perform elementary video processing.

REFERENCES

[1] XILINX, Inc.: *Audio/Video Connectivity Solutions for Virtex-5 FPGAs Reference Designs for the Broadcast Industry: Volume 2 [XAPP1014].*2009, 636 s.

[2] Texas Instruments, Inc.: *Texas Instruments: 3 Gbps HD/SD SDI Adaptive Cable Equalizer [LMH0344 Datasheet].*

[3] BOGATIN, Eric: *Signal and power integrity - simplified, 2nd ed.* Upper Saddle River, NJ: Prentice Hall, 2010, xxvi, 757 s. ISBN 978-013-2349-796.