DC/DC CONVERTER USING FAST-SWITCHING COMPONENTS

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Abstract: Study and implementation of a DC/DC converter operating at high frequency is presented in this paper. The converter is based at Silicon Carbide (SiC) components, which are an excellent opinion (however very costly) if high-frequency switching is required. Fast-switching transistors, inter alia, have fast transients and thus gate driver quality requirements are considerable. Therefore gate driver design is also discussed in the article.

Keywords: DC/DC converter, Silicone Carbide, gate driver, high frequency.

1. INTRODUCTION

Design of a full bridge converter is the aim of the project. The converter, based at Silicon Carbide (SiC) components, is designed to output power up to 4kW at switching frequency of 100kHz. SiC normally-off JFET transistors SJEP120R063 by SemiSouth are used as power switches. JFET transistor is not common for the full bridge topology. SiC JFET transistor has low switching and conduction losses but has higher demands on gate driver and electromagnetic compatibility. There are several commercially available gate drivers on the market but they are usually very expensive. SemiSouth produce gate driver SGDR600P1 which is suitable for SJEP120R063 transistor but the price is enormous (nearly €130 without supply). Therefore a gate driver design is the main goal of the project.

2. POWER PART

As mentioned above, SiC normally-off JFET transistor SJEP120R063 is used. The transistor has breakdown voltage 1200V, continuous drain current 40A and drain-source on resistance 0,063Ω [3]. But it is necessary to use a flyback diode because there is no intrinsic body diode in the JFET structure. Therefore SiC power schottky diode SDP30S120 is used as can be seen at figure 1. The diode has breakdown voltage 1200V and forward current 46A, which are similar parameters as the SiC transistor. The converter is design to be supplied by a DC laboratory power supply only. Thus the DC bus can be directly connected to terminals (without a rectifier or an input filter). There is no need to measure current or voltage because the converter is designed for laboratory use only.

Because of a leakage inductance of the PCB, a low power RC snubber across the DC bus is added to reduce a ringing. Small capacitor 3.3nF placed across gate and source of each JFET is used to eliminate short-through in bridge configuration. The action of turning on one of the JFETs results in a corresponding miller effect on the gate driver of the other JFET. Such it can be transiently turned on as well resulting in excessive switching losses on both devices. Therefore it is better to add more safety margin to slow down the switching action.

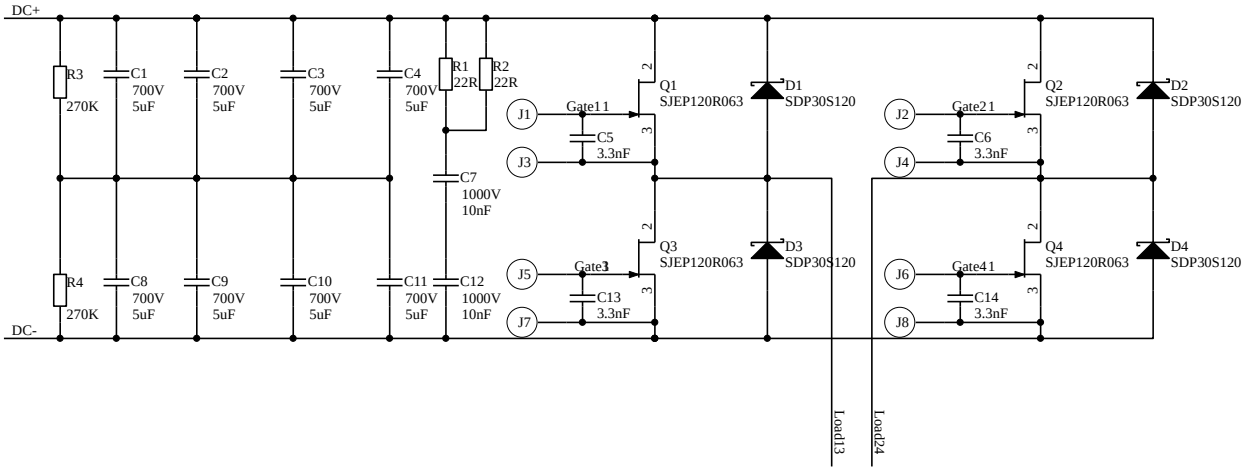

Figure 1 Power part of the converter

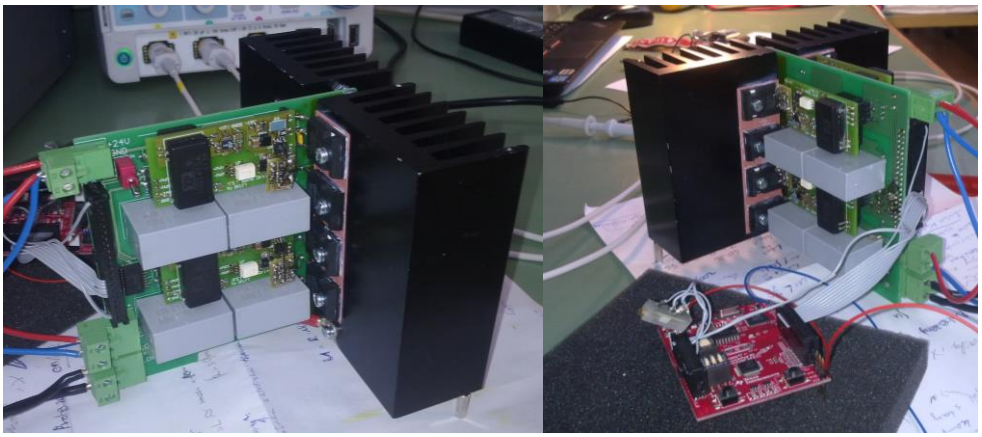

Figure 2 The full bridge converter

2.1. HEAT SINK / COOLING

Heat sink of the converter is designed to minimize parasitic capacities between the heat sink and SiC components. In [1] is shown that a proper handling of parasitic effects is crucial for exploiting the full potential of SiC devices. The capacitive coupling between JFETs and heat sink significantly deteriorates the switching performance of the fast SiC JFETs. Based on results of [1], two separate heat sinks are used. Fully functional converter can be seen in figure 2.

3. CONTROL STRUCTURE

The converter is controlled by an evaluation board C2000 Piccolo LaunchPad. The board is based on a digital signal controller (DSC) Piccolo TMS320F28027 by Texas Instrumental. A Unipolar PWM for DC/DC full bridge topology is generated in the DSC. The program flowchart can be seen in fig. 3a. DSC features such a PWM time base, PWM complementarity, PWM dead time period, synchronization of PWM channels, setting of interrupt, triggering of ADC etc., are adjusted in the initialization section. Then the program enters an infinite loop. Once per PWM period, the program jumps to ADC interrupt service routine where ADC is read and setting of PWM values is performed.

Final signals at gates of the transistors are shown in figure 3b. The figure shows principle of PWM generation which is implemented in DSC. CMPA register determines duty cycle value. The converter is fully on or switched off if the duty cycle is higher than 0.95 or lower than 0.05 respectively.

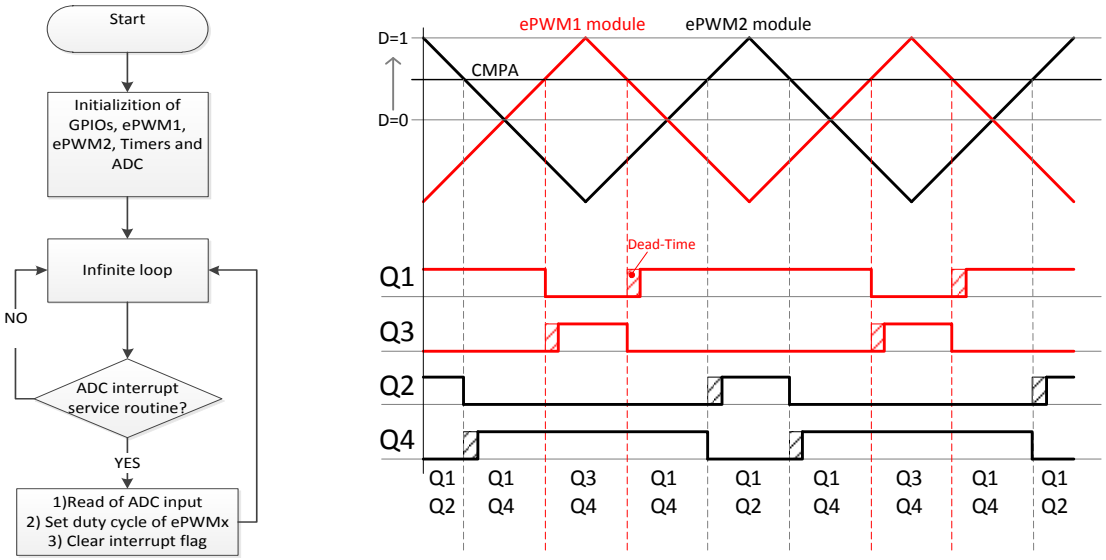

Figure 3 a. program flowchart b. PWM generation process

4. JFET GATE DRIVER

Gate driver is the most important and the most complex part of the converter. There is several ways to control normally-of JFET transistor but all of them are complicated and expensive in comparison with gate drivers for conventional MOSFETs.

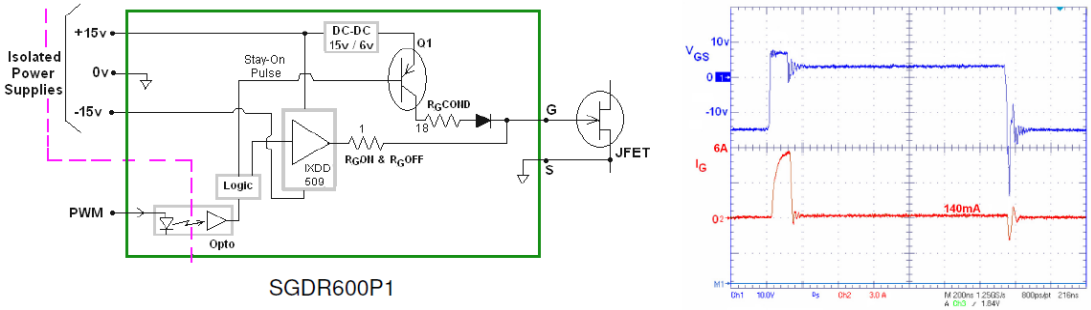

Figure 4 a. Gate driver principle b. Gate waveforms [2]

There are many advantages of the gate driver SGDR600P1 but the price is high. Four-layer PCB cost almost €130, without power supply! It means that the price of complete gate driver, consist of isolated DC power supply with output voltage of ±15V and the gate driver board, can reach up to €200. That price is large portion of the converter price. Therefore, it was decided to build a similar gate driver but cheaper if possible.

4.1. DESIGN OF COMPLETE GATE DRIVER

Gate driver evaluation board SGDR600P1 is recommended for high-speed, hard switching of the transistor SJEP120R063. The SGDR600P1 is an opto-isolated, two-stage gate driver with a single output. The gate driver provides a peak output current of +6/-3A for fast turn-on and turn-off transients with low switching energy losses.

The design of our gate driver has only a few differences but from the functional point of view, it is the same gate driver as SGDR600P1 (fig. 4). The gate driver is designed to apply a high peak current pulse for fast turn-on of the transistor. The current pulse, generated by IXDD609, can achieve up to 6A and is optimized to minimize power losses. Thus duration of the pulse is limited to 100ns. The fast turn-off is also provided by the IC driver IXDD609, which has the sinking ability (provides negative gate voltage of -15V). PNP transistor Q1 is switched to maintain the steady state

gate current of 140mA, required to sustain gate-source channel open with low losses. The PWM signal enters to logic block, which generates a new PWM signal, synchronized with the original one but shorter and inverted. The original PWM signal controls Q1 transistor. The modified PWM signal goes to an enable input of the driver. It is the way how the gate waveform (fig. 4b) is made.

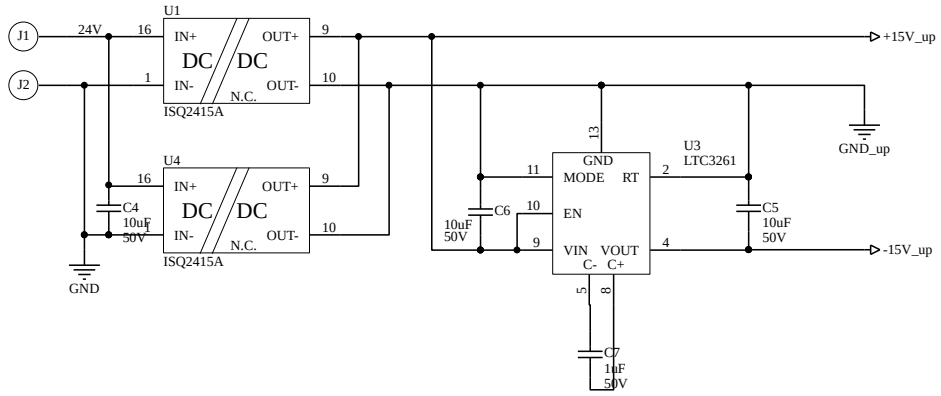

Figure 5 Galvanic isolated supply for the gate driver

Galvanic isolated power supplies have been designed on a common PCB with the gate driver (fig. 6). Two 2W DC/DC converter ISQ2415A with 24V input voltage, 15V output voltage and 10pF isolation capacitance are used as the main isolated supply (U1, U4). Necessary negative voltage -15V is made by inverting charge pump LTC3261 (U3). Schema of described supply is shown at figure 6. Energy consumption of the gate driver is calculated to a maximal of 3,5W (for upper transistor switched with high duty cycle at 100kHz). Most of the energy is consumed when the power transistor is turning-on (6A peak) and also during conduction period of the transistor (140mA through resistor R_G). Consumption of the gate driver during turning-off and off-state of the transistor is only a few milliamps in average. Therefore the charge pump LTC3261, which has maximal output current 100mA, can be used without worries.

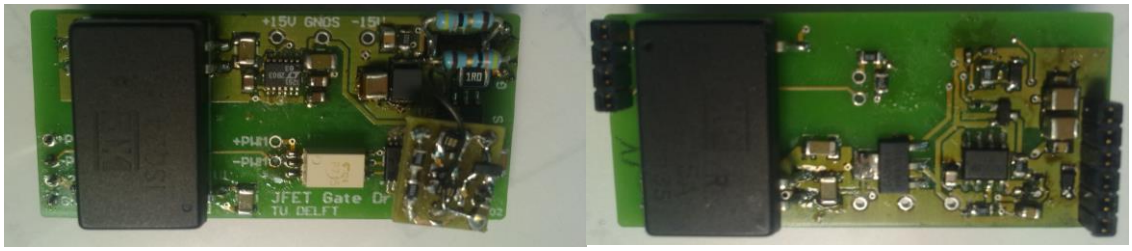

Figure 6 Described gate driver. Left: top, right: bottom

5. MEASUREMENT

The Converter was built and measured. A laboratory power supply was used to provide DC bus voltage. The converter was tested and results of performed measurements are presented.

GS voltage and gate current waveforms of the transistor Q3 are shown in figure 7. Gate current is slightly more rippled which is caused by measurement error (There is lack of space and thus the gate current was measured by Rogowski coil). Rise time is 19ns and fall time is 30ns.

Waveforms of GS and DS voltage of the lower transistor Q3 are shown in figure 8. There is also captured the load current which reaches 4,8A in average. Considerable ringing can be observed on the GS voltage signal. However the rising and the falling edge of DS voltage can be considered as fast and stable without any potential interferences or glitch. The rising time of DS voltage is about 60ns and the falling time of DS voltage is 25ns, which are very satisfactory results.

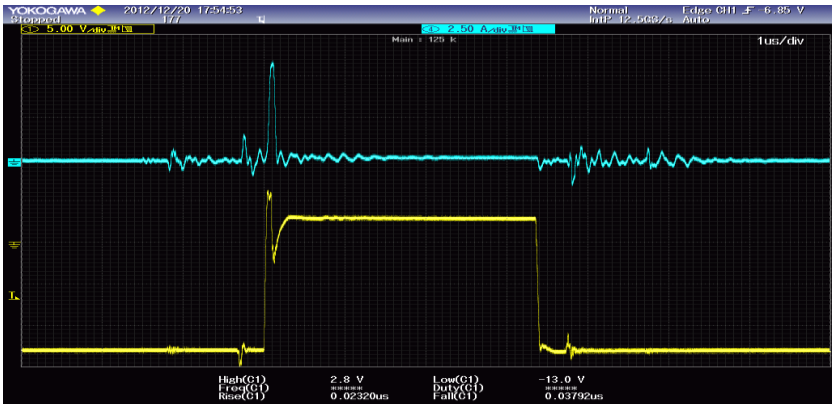

Figure 7 Proposed gate driver waveforms of GS voltage (yellow) and S current (blue), DC bus voltage 540V

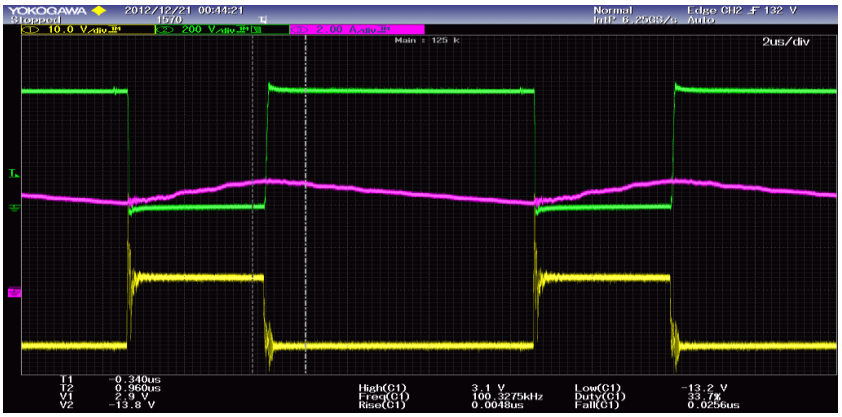

Figure 8 Upper transistor Q3 waveforms of GS voltage (yellow), DS voltage (green) and load current (purple), DC bus voltage 540V

6. CONCLUSION

Design and production of the full bridge converter using SiC JFETs and its gate driver are described in the article. The converter has been designed to minimize parasitic parameters and therefore great emphasis was placed to the design of the PCB and the cooling. The result is small dimensions of PCB as well as relatively nice waveforms of main parameters with small interference.

The proposed gate driver has the same features as the gate driver evaluation board SGDR600P1. The gate driver PCB is compatible with the PCB of SGDR600P1. Furthermore it contains pretty quality isolated power supply.

Basic measurement was made. Waveforms are stable and satisfactory. Transients are fast and without significant interference. The converter is good basis for further work. Power part is universal and converter features can be easily modified in the program of DSC if necessary.

REFERENCES

[1] Josifović, J. Popović-Gerber, J.A. Ferreira: “SiC JFET Switching Behavior in a Drive Inverter under Influence of Circuit Parasitics”, 8th International Conference on Power Electronics, 2011 (ICPE 2011)

[2] www.SemiSouth.com - Datasheet of SGDR600P1 gate driver evaluation board avaliable online

[3] www.SemiSouth.com - Datasheet of SJEP120R063 normally-off Silicon Carbide JFET avaliable online