THE NETWORK CONNECTION OF THE FPGA DEVICES

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Abstract: This paper deals with design of the network connection between two development boards ML505 using FPGA devices Virtex-5. FPGA devices are programmed in VHDL (VHSIC hardware description language) language in the ISE Xilinx software. Data are sent in UDP (User Datagram Protocol) datagrams. UDP datagrams are sent to the PC (personal computer) in the first step, where UDP datagrams are received and checked in the Wireshark programme. After the successful connection of FPGA with PC, two FPGA devices are connected together.

Keywords: Network connection, FPGA, VHDL, UDP datagrams, Xilinx ISE

1. INTRODUCTION

FPGA Virtex-5 is installed on the development board ML505, where the network connection is realized with one gigabit per second (Gbps) speed. Programmable system clock generator creates 125 MHz clock signal for GMII Ethernet physical interface. The control of the GMII interface is programmed in the Xilinx ISE programme, where is IP Core created. It is called Tri-mode Ethernet MAC wrapper. The control is very effective when the IP core is used. UDP datagrams was sent from the network interface. These UDP datagrams was created in the next VHDL module. For successful communication, the UDP datagrams was sent to the PC, where they were checked in the Wireshark programme. Afterwards, UDP datagram can be sent to the second development board, where the same programme is implemented as on the first development board.

2. UDP DATAGRAM

The UDP protocol realizes an unreliable service. The PC or some other device can send UDP datagram to the other PC or device without creating a connection. This communication is not reliable. The receiver does not confirm UDP datagram reception and the sender does not know if the datagram was delivered. The header of the UDP datagram is inserted to the IP header and both are inserted to the header of the Ethernet frame. The header of the Ethernet frame is very simple and contains MAC address of source, MAC address of destination and the next protocol, which is the last in the header of the Ethernet frame. IP protocol is used in this case. The array has value 800 in hexadecimal notation. The IP header is more difficult and contains a lot of information, for example version, header length (20 byte), time of live, fragmentation and source and destination IP addresses. There is a UDP header after the IP header. It contains source and destination port and length of the UDP datagram. The minimum length behind the Ethernet header is 46 bytes. The IP header has only 20 bytes and the UDP header has only 8 bytes. The minimum data payload is thus 18 bytes. [1] [2]

3. DEVELOPMENT BOARD ML505

The development board ML505 contains FPGA Virtex-5. There are a lot of additional devices like the network interface and buttons. The buttons are used for selection of the result character and this

character is sent via network interface to the next equipment, like the PC or another development board. The development board ML505 is shown in Fig. 1.

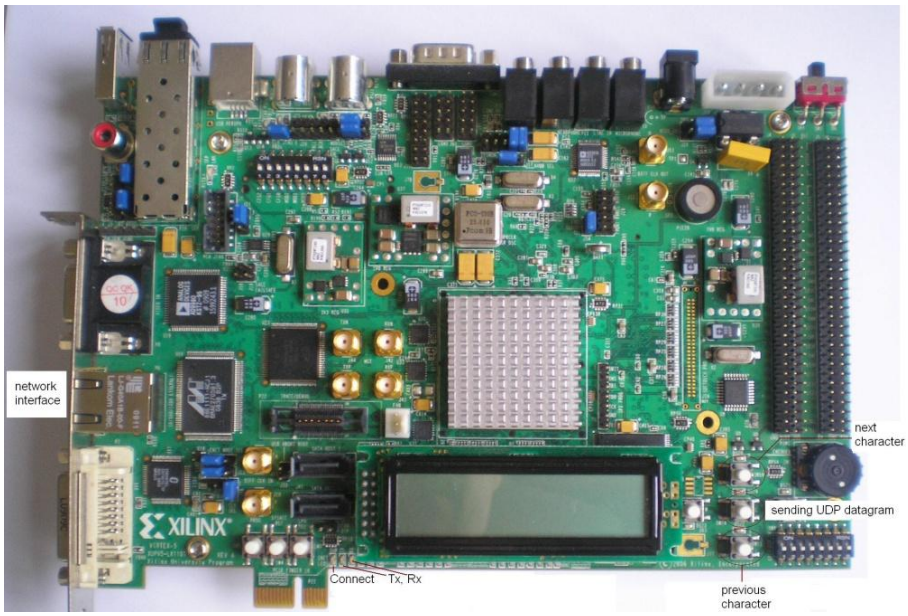

Figure 1: Development board ML505

4. NETWORK CONNECTION WITH PC

The FPGA device is programmed with VHDL language in the Xilinx ISE software. The top unit is the schematic in a new project. There are three VHDL modules in the schematic. The complete software design is created with these three VHDL modules. The result of the schematic is shown in Fig. 2.

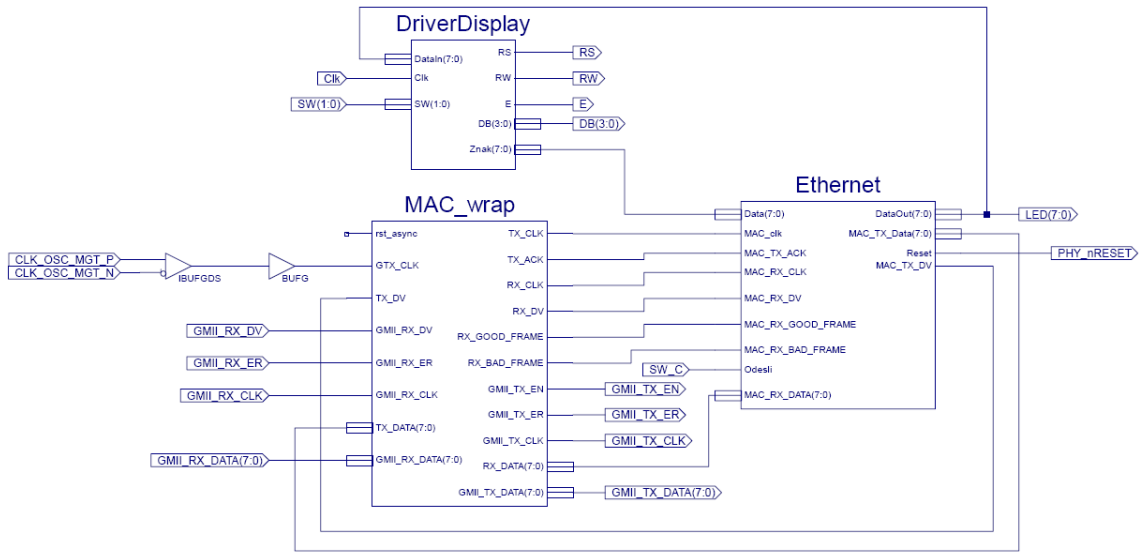

Figure 2: The final design in ISE Xilinx

The VHDL module called MAC_wrap has a control over the physical network interface and it is created by IP core. Only one IP core is used in this project. The input clock signal is created in the programmable system clock generator and the frequency of the clock signal is 125 MHz. Maximum frequency reported by the Post-PAR static timing report is 133.280 MHz. The schematic used 1 % LUT in the FPGA Virtex-5. The UDP datagram is created in the VHDL module called Ether-

net. The last VHDL module is called DriverDisplay and it implements a driver for the LCD display. There are three control signals and four data signals. The buttons are connected to this module and the final character is selected on the LCD display. This character is sent via output signal called Znak to the Ethernet module, where UDP datagram is created with this data. Complete UDP datagram is sent to the MAC_wrap module and this module send the data to the network interface. The LCD display is a part of the development board ML505. The UDP datagram is sent to the PC in the first step, where it is checked in Wireshark software. The received datagram is shown in Fig. 3.

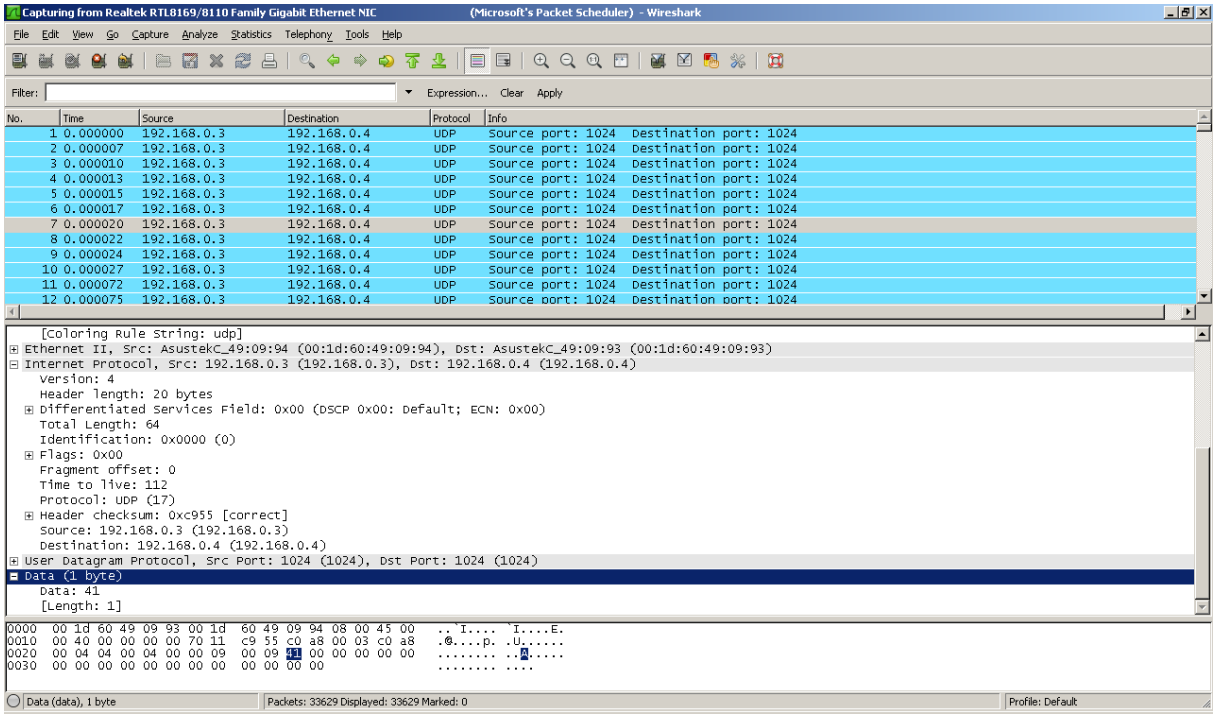

Figure 3: Datagram in the Wireshark software

The Ethernet frame is shown in the Wireshark software. There is a MAC address of source in the beginning of the Ethernet packet. After the MAC address of source there is a MAC address of destination. The MAC address of source is the MAC address of the FPGA device increased by one. After MAC addresses there is a definition of next protocol, which is the IP protocol. This is the reason why there is a hexadecimal value of 800. The header of IP protocol has 20 bytes. There is a lot of information, for example time to live, IP addresses and information about segmentation. A point-to-point network was created by the connection of PC with FPGA. IP addresses are in class C networks. There is a UDP header after IP header. The UDP header contains the length of datagram and the values of port, which is 1024. There is only a value of character in the data payload, which was previously set on the LCD display. The character A is shown in the Figure 3. The minimum data payload is 18 bytes, but there is only one effective byte. This is the reason why there are 17 zero bytes at the end of the Ethernet frame.

5. NETWORK CONNECTION FPGA DEVICES

After the test of successful connection between the FPGA and PC, two FPGA devices have been connected together. FPGA devices have implemented the same code. The network bridge can be realized in this way. The UDP datagrams are sent after pushing the button, which is on the development board. This situation is shown in Fig. 4.

Figure 4: Setting up an H character and sending

The communication is shown in Fig. 4. The button for sending the UDP datagrams is pushed. LED diodes for network connection and transfer of the character are actived. The H character is transferred in this case to the second development board, where it is received and displayed on the LCD display. This situation is shown in Fig. 5.

Figure 5: Character H is received

The complete realization of the network bridge is shown with the development boards ML505 in Fig. 6.

Figure 6: Network bridge

6. CONCLUSION

A gigabit network connection UDP datagrams was realized in the Virtex-5 FPGA. UDP datagrams were sent to the PC in the first step, where UDP datagrams were checked. After successful communication of FPGA device with PC, the network bridge with two FPGAs was created. The development boards ML505 were used in this project. The final connection is shown in the figures. UDP datagram can contain a lot of effective bytes in the future.

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