FPGA BASED DATA AQUISITION SYSTEM

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ABSTRACT

Even though the market with various systems for measurement and data acquisition is very rich, there are many applications where development of new single-purpose system becomes necessity. This paper describes one of them. Requirements on high number of input channels, but quiet simple functionality made commercially available equipment too expensive. Because of requirement on very short development time modular architecture based on FPGA development kits was chosen as a solution..

1. INTRODUCTION

Even though the market with systems for measurement and data acquisition is very rich, there are many applications where development of new single-purpose system becomes necessity. Simple, available and cheap equipment usually doesn't allow user to adjust functionality for their exact needs and its scalability is also limited. More complex and flexible systems become more expensive and their price grows very fast with their size. In our case, requirements on high number of input channels, but quiet simple functionality made commercially available equipment too expensive. Also very short time for development was limiting factor.

Modular architecture based on FPGA development kits was chosen as a solution. FPGA architecture offers us flexibility that is necessary for both input circuitry development and interconnecting with other modules of the system. FPGA development boards are often equipped with high number of input pins and they are easily available for reasonable price.

2. TECHNICAL REQUIREMENTS ANALYSIS

Main purpose of the system is collecting data from 288 input channels divided into 6 groups; transfer it into personal computer and save it to disc in form of textual records. Input signal is defined as impulse signal with impulse width from 0.1 us to 1.0 us. In the further text each impulse is called an event. Each group of inputs can receive approximately 100 thousands of events per second during measurement. Events can come independently on any input channel at any time. There can be fluctuations in event rate received by the group so we designed system to be able to cope with at least twice the given average event rate what was agreed by the customer as a reasonable reserve.

For each event, timestamp, pulse width and channel identification was required to be collected. Resolution of the timestamp and pulse width measurement was required at least 20 ns (sampling rate 50 MHz). Timestamp length is 32 bits, pulse width length is 8 bits, and channel identification number was selected as 8 bits long as well. According to this specification each event generates 6 bytes of data. When event leaves group of input channels next identification has to be added. Group identification number is also 8 bits long. With next 8 bits reserved for future purposes and state flags, we get 8 bytes generated for each event.

Another requirement was to have possibility of collecting data for at least 45 minutes and storing data on personal computer.

3. SOLUTION

As mentioned above modular architecture based on FPGA development kits was chosen for solution. System was divided into three layers – acquisition, concentration and data storage layer. Figure 1 shows us an overview of the whole system structure.

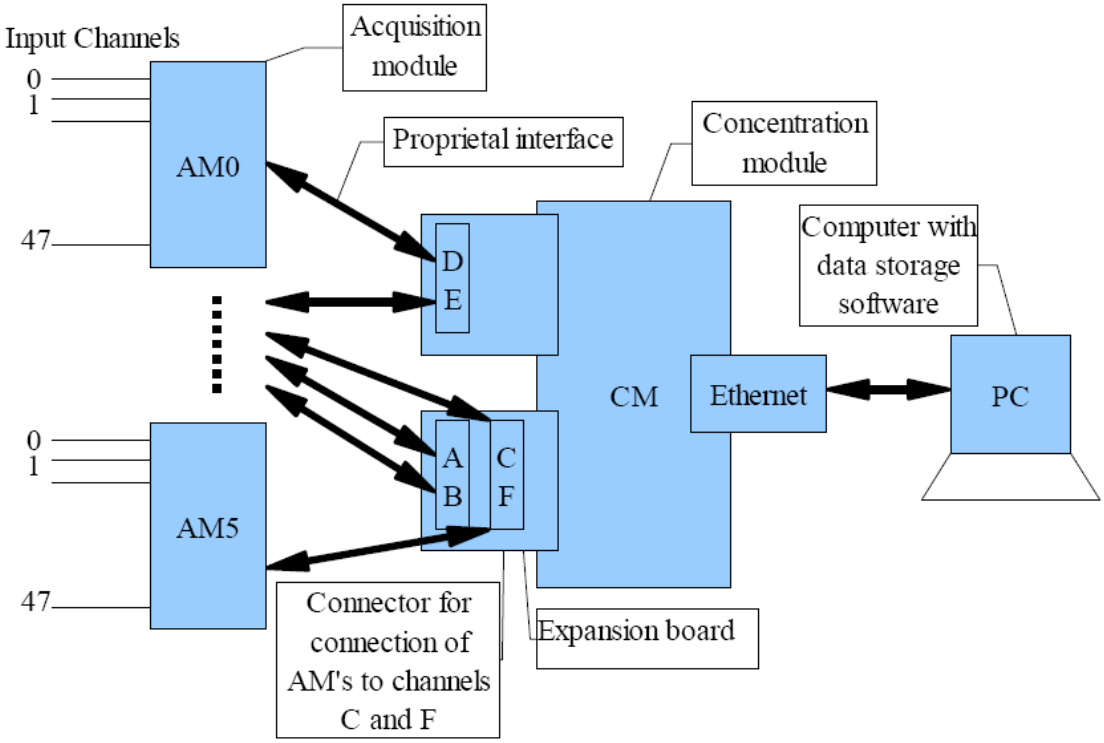

Figure 1. System block scheme

3.1. ACQUISITION LAYER

The acquisition layer is responsible for acquiring data from digital inputs and passing it to concentration layer. This layer consists of six Cyclon III starter board kits [1] with 48 digital inputs each (six acquisition modules AM0 to AM5). Each AM collects data form one input group.

FPGA design contains 48 identical units that monitor one input each. When rising edge is detected timestamp is registered and pulse width counter is started. When falling edge is detected, pulse width is registered and timestamp, pulse width and channel ID is put into FIFO as one 48 bit wide word. Pyramidal structure of FIFOs ensures that event records from all inputs are transferred into one FIFO on the top.

Another part of AM is communication interface used to connect AM to concentration module. It takes data from above mentioned FIFO and sends it through 8 bit parallel bus to concentration module. This interface consists of 13 signals. Eight of them represents data (DATA7-DATA0), one signalizes valid data on the bus (FRAME), one signalizes beginning of the frame (START - active only when valid first byte is on the bus), reset signal (RST) used to synchronize all boards (timestamps), 10 Mhz clock signal (SYS_CLK) that is used by AM as a clock input, 10 MHz clock signal (CLK) that is generated by AM – CM samples all other signals on the rising edge of this clock.

The AM/CM interface is designed to be able to transfer 200 thousands of event records per second. Each byte of frame needs 6 clock cycles to be sent. At least two clock cycles are interleaved between each two frames as a gap without valid data. Half of data lines change state in the first clock cycle of each byte transfer, the other half changes state in the second clock cycle. This technique is used in order to reduce interference and crosstalks on the bus. Next waveform (figure 2) demonstrates one frame transfer.

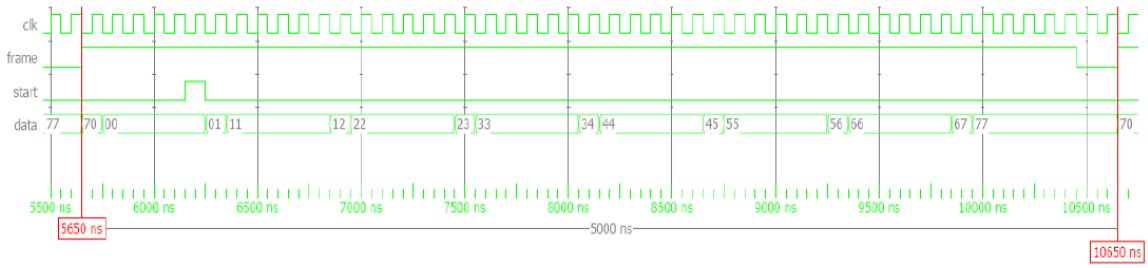

Figure 2 AM/CM communication interface waveform

3.2. CONCENTRATION LAYER

The concentration module is implemented in Stratix II GX PCI Express Development board [1]. CM supports 6 input channels for AM's. Design can be divided into three layers. The first one is layer of interfaces that receive data from AM's. For each channel one receiver is implemented in the FPGA design. Each one is considered as independent clock domain. Received data are stored in FIFO's. Each receiver has its own FIFO for received data. The second layer merges data from FIFO's of all receivers into one FIFO (merged data FIFO). Events are copied from receivers FIFO's to FIFO with merged data on round-robin basis.

The last layer is responsible for packing data from merged data FIFO into broadcast UDP packets. Packet is sent on the line as soon as merged data FIFO contains 160 event records. 16 byte header is added on the beginning of each packet. Payload of each packet contains 1296 bytes of data. Second and third layer have their own clock domain running on 125 MHz. This clock is generated by PLL from 100 MHz external oscillator as well as 10 MHz clock that goes to AM's.

3.3. DATA STORAGE LAYER

Data storage layer is a simple PC application that receives UDP packets form the Ethernet network, stores it and decode it into textual records.

3.4. CLOCK DOMAINS IN THE DESIGN

The figure 3 shows the overview of the clock domains of the system. To keep all time-stamps in all modules synchronous, all modules must be fed with the same clock. Frequency of this clock had to be chosen with respect to used wiring and PLL limits 10 MHz (system clock). AM consists of two clock domains. One consists of communication interface and runs at system clock. The second consists of input channels and runs at sampling frequency (e.g. 50 MHz).

CM consists of six clock domains running on clocks from AMs (may be phase shifted) and one clock domain running at 125 MHz consisting of ethernet interface.

Reliable data transfer between clock domains is ensured by FIFOs.

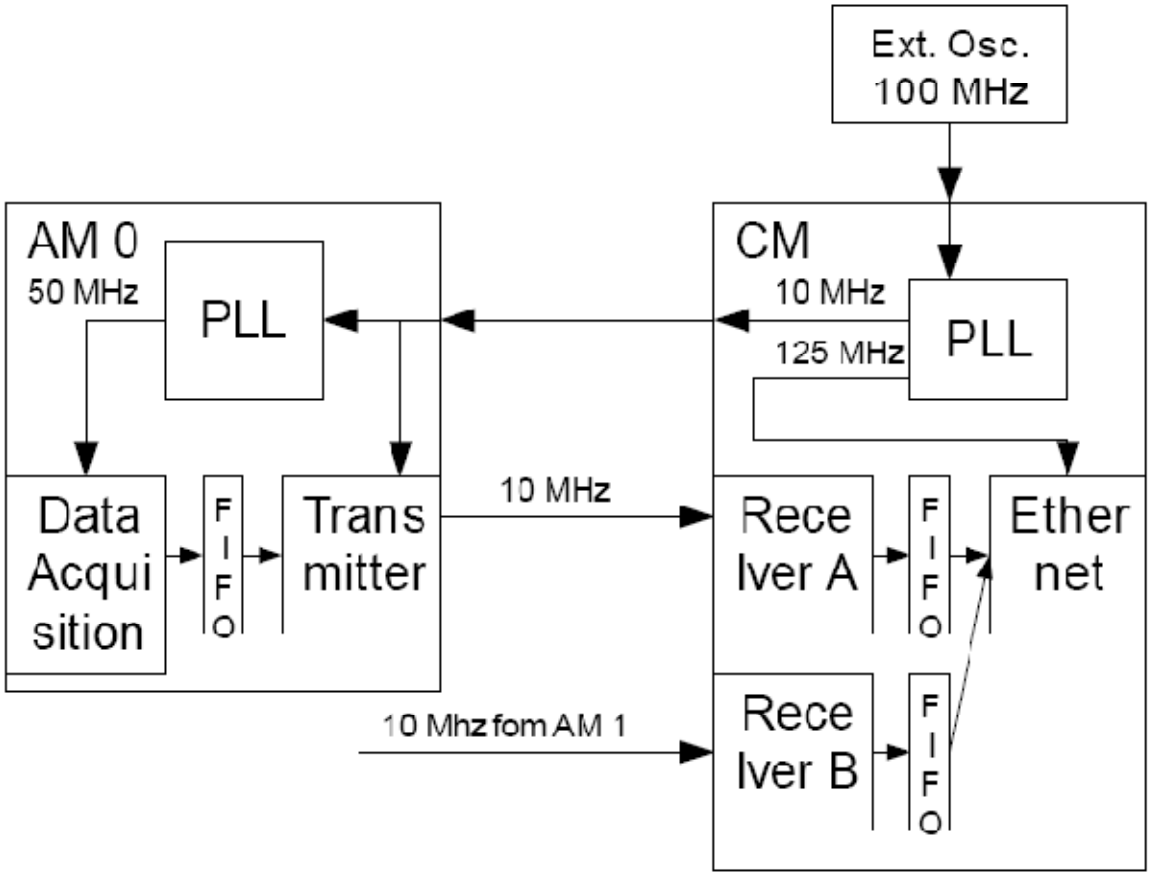

Figure 3 Clock Domains of the design

3.5. ETHERNET INTERFACE

Gigabit ethernet interface was chosen for data transfer from CM to PC. Because system will never work in open network or Internet, we can use simple broadcast communication

using UDP protocol. Communication is unidirectional what further simplifies needed hardware.

Communication is ensured by simple core in FPGA that sends broadcast UDP packets. To simplify necessary core as much as possible we can send packets with predefined data amount only. Such packets can have constant all headers (ethernet, IP, UDP), only ethernet CRC [2][3] has to be adjusted for each packet.

Ethernet core is connected to FIFO that holds merged data from all AMs. As soon as 160 events is available in the FIFO (1280 bytes) 16 bytes of user information (number of packet, user flags etc.) are added and one packet is send. Maximal throughput of this interface is near to 100 MB per second what is much more then data throughput required by the application (10 MB/s).

4. CONCLUSION

This paper described design of data acquisition system that is able to collect information about impulse signals form up to 288 input channels and transfer it over Ethernet network to personal computer. Whole system is based on FPGA development boards what enabled rapid development of this system with keeping price low.

ACKNOWLEDGEMENT

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