FULLY-DIFFERENTIAL T/H CIRCUIT BASED ON MILLER CAPACITANCE

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ABSTRACT

Track and Hold circuits are widely used in signal processing and data conversion systems. High resolution analog-to-digital conversion modules require T&H-circuits for track-and-hold and deglitching. Track and Hold circuits can cause various types of signal degradation. The design philosophy of sample and hold (or T/H) circuits requires a careful consideration of each possible error source. Also quality aspects such as mismatching properties of active and passive devices must be taken into account during the design. This text is dealing with advanced T/H circuit using fully-differential topology, which is based on Miller capacitance.

1. INTRODUCTION

The track-and-hold circuit finds extensive use in data converter applications as a sampling gate. A variety of topologies exist, each with their own benefits. The simplest one is created by hold capacitor and NMOS transistor as a switch.[1] This circuit suffers from the clock feedthrough and charge injection problems. The foundation for new topology is conventional Miller-capacitance-based T/H circuit [4] seen in fig.1.

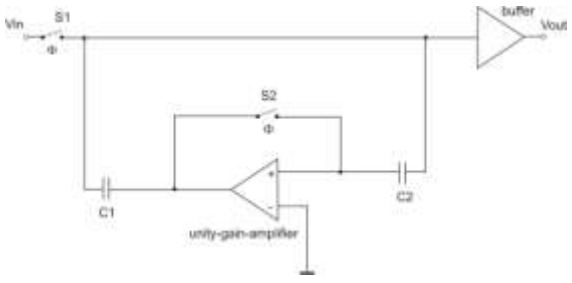

Fig 1: Conventional Miller-capacitance-based T/H circuit, reference [4]

The conventional Miller-capacitance-based T/H circuit consists of an input sampling switch S1, the Miller feedback circuit, and a high input-impedance unity-gain buffer. The Miller feedback circuit is made up of two capacitors (C1 and C2), the switch S2 and an operational amplifier. In the sampling mode, both S1 and S2 are closed, The operational amplifier is configured as a unity gain circuit. It means that it only provides virtual ground at the input and output nodes of the op-amp.

2. ANALYSIS

2.1. FULLY-DIFFERENTIAL T/H CIRCUIT BASED ON MILLER-CAPACITANCE

If we use instead the simple operational amplifier fully differential operational amplifier, we can extend the topology as seen in the fig 2.

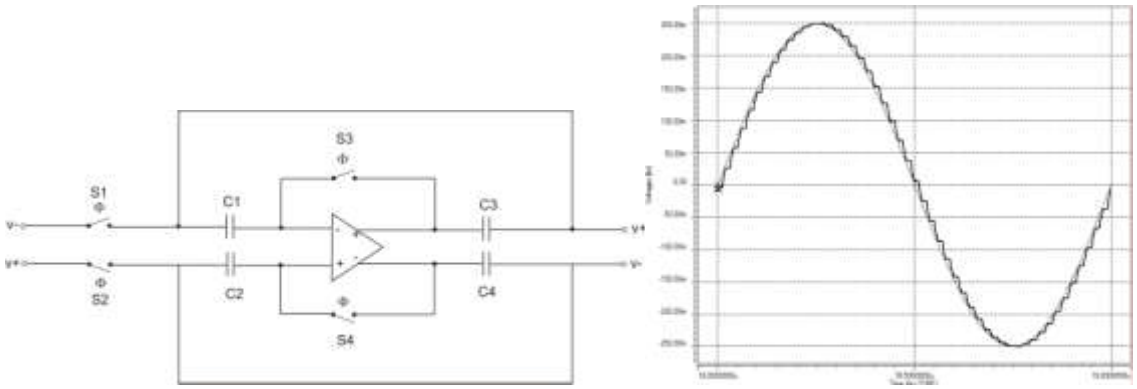

Fig 2: Fully differential T/H circuit on the left, Illustration of the T/H circuit output performance on the right

When the switches S1 and S2 are closed (on), the input signal is transmitting to the output (track-mode) , at the same time the capacitors C1 and C2 is charging up. At this moment, the charge injection and clock feedthrough effects appear as a common-mode signal to the amplifier and they are reduced by the CMRR of the amplifier.

The final topology of the differential OTA with buffer is seen in fig 3. The transistors M18 – M21 create the buffer for both outputs.[3] The buffer does not invert signal from its M21´s (M20´s) drain-input to the output of the OTA even if it is inverting amplifier in itself. This means that the inverting and non-inverting outputs of the OTA remain the same as in the previous case without buffer.

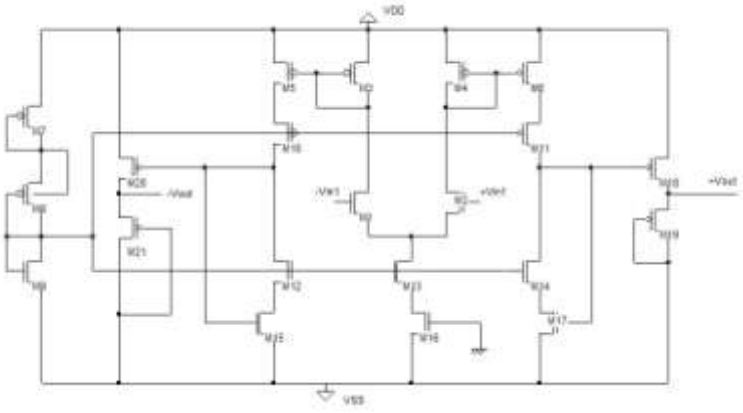

Fig 3: Balanced OTA with buffer,references [1],[2],[3]

Table 1 shows results from the corner analysis. The corner analysis was made with output load R = 10kΩ and C = 5nF . For this values are the following results presented.

ota with buffer	typ N-P	slow N-P	fast N-P	N slow P fast	P slow N fast
Iss (uA)	210,4	133,7	347,7	234,6	199,4
gm (uA/V)	550	408	739	516	595
gain	9,61	13,7	6,05	10,5	7,8
BW (MHz)	1,16	1,03	1,36	1,24	1,13
GBW (MHz)	11,1476	14,111	8,228	13,02	8,814
Input range (mV)	490	410	500	350	330
power supp. (V)	2,7	2,7	2,7	2,7	2,7

Tab 1: Results of the corner analysis, technology Amis 0.35µm

When the S1 and S2 are open, the charge from the capacitors C1 and C2 is transmitting through the C3 and C4 to the output (hold-mode). As a switch is used a simple transmission gate made from two transistors NMOS and PMOS.

The sampling frequency in illustration (fig 2 – right) is 50MHz and the frequency of the input signal is 1MHz with the amplitude 0,5V. The maximum error can be expressed

$$INL_{MAX} = \frac{1}{2} LSB \tag{1}$$

$$LSB = \frac{V_{ptp}}{2^n} \tag{2}$$

Where V_{ptp} is the voltage range of the signal and *n* is the number of the bits. Now we can express an equation for calculating *n* if we know the error value.

$$n = \log_2 \frac{V_{ptp}}{LSB} = \log_2 \frac{V_{ptp}}{2INL_{MAX}} = \frac{\ln \frac{V_{ptp}}{2INL_{MAX}}}{\ln 2} \tag{3}$$

Example from the circuit. The V_{ptp}= 1V , INL_{max} = 0,88mV, then

$$n = \frac{\ln \frac{1}{2 \cdot 0{,}00088}}{\ln 2} = 9{,}149 bitů \tag{4}$$

The result would be 9-bit resolution. The following table 2 shows the results from the simulation of the errors. For the simulation were used capacitors C1-C4 with values 1,5pF. There are n-bit resolution for different sampling frequency, input signal frequency and voltage range in the table.

Sampling frequency	**50 MHz**			
	signal frequency			
input range	**50kHz**	**100kHz**	**500kHz**	**1MHz**
0,5 V	8bit	8bit	8bit	8bit
0,75 V	8bit	8bit	8bit	8bit
1 V	9bit	8bit	8bit	9bit

Tab 2: Simulation results

As is seen, the circuit is possible to use for 8-bit converter. The final performance of this sample-and-hold circuit is illustrated in table 3.

power supply	2,7V (±1,35V)
total power dissipation	151,45mW
number of output bits	8
max. input range	1V (±0,5V)
sampling frequency	50MHz
max. input freq.	1MHz

Tab 3: Summary of the results

Power dissipation is due to the big buffer in the operational amplifier. If we decrease the dimensions of the transistors in the buffer, the power dissipation will decrease too. But the bandwidth of the OTA might be then less than 1MHz

2.2. PROPOSED LAYOUT

The layout is designed in technology 0,35µm AMIS.

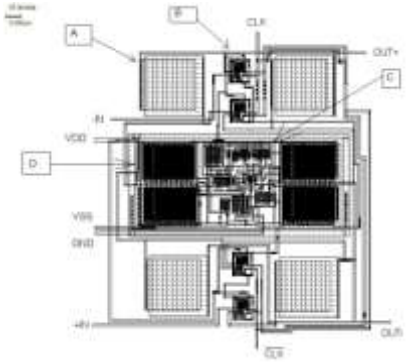

Fig 4: Final layout structure

„A“ is pointed to the capacitors. The capacitors are made from poly1 and poly2 layers and their size is determined by the value of 1,5pF. It is possible to calculate it with help of the equation (5)

$$1{,}1 \pm 0{,}15 \ \text{fF}/\mu\text{m}^2 \qquad (5)$$

„B“ is pointed to the switches, which are impact between the capacitors. „C“ shows the operational amplifier and „D“ the output stage of the amplifier – buffer. „Guard ring“ surrounds whole operational amplifier with buffer . Also each switch is surrounded by „guard ring“.As a complex has the layout 9 output pins as is seen in fig.5. The final area of this layout is 36 400 µm2.

3. CONCLUSION

Track-and-hold (T/H) circuit is an important analog building block that has many applications.The simplest T/H circuit can be constructed using only one MOS transistor and one hold capacitor. However, due to the limitations of the MOS transistor switches, errors due to charge injection and clock feedthrough restrict the performance of T/H circuits. As a result, different T/H techniques and architectures are developed with the intention to reduce or eliminate these errors. Best way to avoid errors is to use fully-differential topology

which needs to have a fully differential operational amplifier. The fully differential topology is convenient for reducing errors which appear during the switching, namely charge injection and capacitive feedthrough. The operational amplifier should reduce the clock feedthrough and charge injection by its common-mode feedback. The summary of the results is seen in table 4.

power supply	2,7V (±1,35V)
total power dissipation	151,45mW
n-bit resolution	8 bits
max. input range	1V (0,5V)
sampling frequency	50MHz
max. frequency of the input signal	1MHz
area in 0,35 um	36 400 μm^2
transistors	29

Tab 4: Final results of the track-and-hold circuit

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