BPSK, QPSK MODULATOR SIMULATION MODEL

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ABSTRACT

This project arised out of the diploma thesis called „BPSK, QPSK Modulator and Demodulator“. Design facilities of the modulator in the FPGA are presented in this paper using a VHDL language and DDS component in the Xilinx ISE development tool. The basic building block is a DDS synthesizer accessible as an intelectual property core. The result is a modulator simulation model with possibility of implementation in FPGA.

1. INTRODUCTION

The digital design was chosen because the advantages of a digital solution are apparent. The main advantages of the digital solution are frequency agility, repeatibility, cost and the simpler reconfiguration compared to analog as I experienced in my diploma thesis [1].

The reason why an FPGA was used is that the FPGA is highly configurable silicon engine, with high MIPS (Mega Instruction Per Second) real-time signal processing functions. Compared to the digital signal processors (DSP), FPGA are characterized by a high flexibility. The revolutionary evolution in FPGA technologies in last years allowed increasing gate count, clock speed and integration of many functions like dedicated high-speed hardware multipliers and embedded processors.

The next chapter presents an analysis of the Phase Shift Keying (PSK) modulation. The following chapter desribes the design of modulator. Next chapter refers to modulator mapping to the FPGA. The last chapter summarizes the whole process from analysis to creating the simulation model.

2. ANALYSIS

PSK is a digital modulation where the carrier phase is keyed by the digital modulation signal. Two types of modulations, the BPSK and QPSK are desribed and used in this case.

In BPSK modulation the carrier phase acquires two discrete states (0° and 180°), which correspond to one bit of the modulation signal. Therefore the symbol period is equal to the bit period $T_s = T_b$. The BPSK modulated output is expressed as:

$$s(t) = m(t).\cos(2\pi f_C t + \phi), \qquad (1)$$

where m(t) is a modulation baseband signal ±1, f_c is a carrier frequency and ϕ is an initial phase.

In QPSK modulation the carrier phase acquires four discrete states (±45° and ±135°), which correspond to a couple of modulation signal bits. The symbol period is twice the bit period $T_s = 2.T_b$. The QPSK modulated output is expressed as:

$$s(t) = m_I(t).\cos(2\pi f_C t + \phi) - m_Q(t).\sin(2\pi f_C t + \phi). \qquad (2)$$

The advantage of these carrier-supressed modulations is decreasing the spectral energetic density, because the carrier energy is not included in spectrum. On the other hand, the design of carrier recovery blocks in receivers is rather difficult.

3. MODULATOR

3.1. DESIGN

In accordance with [2], the modulator consists of two general parts, as shown in **Fig. 1**. There are a baseband modulation signal processing block (Symbol mapper) and a carrier generation block (DDS synthesizer) with multipliers.

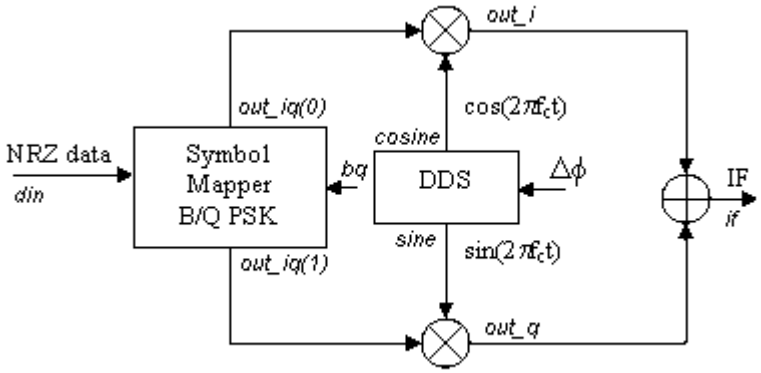

Fig. 1: Block diagram of modulator.

Symbol mapper switches the modulation type (BPSK, QPSK). In QPSK case every couple of bits is divided into two channels I and Q. The odd bit goes to the I channel and the even bit goes to the Q channel. Otherwise in BPSK case the whole dataflow goes to I channel and Q channel is unplugged.

The most important part of the modulator is the Direct Digital Synthesizer (DDS) [3], which generates two quadrature carrier waves. The DDS is used for generating waveforms by LUT tables, where the samples of a harmonic function are stored. Samples may be stored either in the distributed memory or in the block memory in FPGA structure. The DDS block diagram is shown in **Fig. 2**.

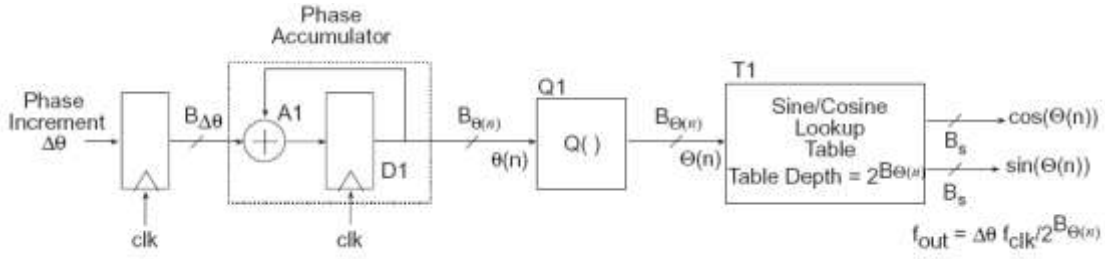

Fig. 2: DDS synthesizer block diagram.

The rest of the modulator is created by multipliers and an adder. Because only the sign of a carrier wave changes in modulator the simple algorithm is used instead of multipliers. It is performed by negation of carrier samples. This block with the output adder and the DDS synthesizer is presented in the VHDL code bellow.

3.2. SIMULATION

A simulation of the symbol mapper function is shown in Fig. 3. Signal *din* is an input dataflow timed by the input clock *clk_b*. Signal *out_iq* is an output of the symbol mapper into the two channels. Signal *bq* switches the type of a modulation (BPSK, QPSK).

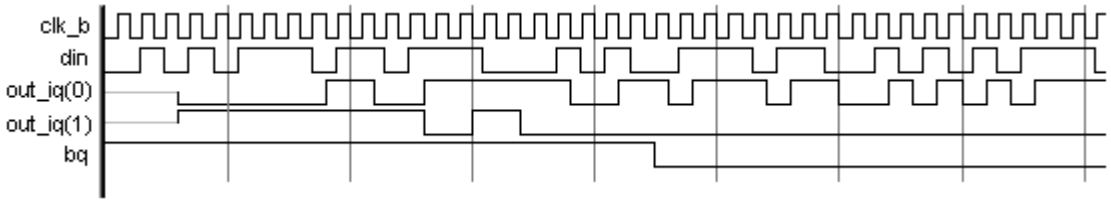

Fig. 3: Simulation of the Symbol Mapper block.

Following VHDL code demonstrates the output part of modulator. As it is shown, the sign of quadrature carriers (*SINE*, *COSINE*) is keyed by modulation signal *out_iq*. It results in two channel signals *out_i* and *out_q*, which are processsed in dependence on type of modulation. The integer conversion shifts the sign bit to the most important bit in the output signal vector *if*, because signal *if* is one bit wider than signals *out_i* and *out_q*.

```
if CLK'event and CLK='1' then
    case (out_iq) is
       when "00" =>
          out_i <=not(COSINE);     out_q <= not(SINE);
           when "01" =>
          out_i <= COSINE;         out_q <= not(SINE);
           when "10" =>
          out_i <= not(COSINE);    out_q <= SINE;
           when "11" =>
          out_i <= COSINE;         out_q <= SINE;
           when others =>
          out_i <= COSINE;         out_q <= SINE;
    end case;
    if bq='1' then
          if<=conv_std_logic_vector((conv_integer(out_i)-
          conv_integer(out_q)),11);
    else
          if<= conv_std_logic_vector((conv_integer(out_i)),11);
    end if;
end if;
```

Simulation results of modulator and demodulator functional models are shown in Fig. 4 and Fig. 5. Signal *out_iq* is a digital modulation signal available on inputs to both channels. Signal *if* presents the modulator output samples. Signal *if* is quantized and interpolated for the better lucidity.

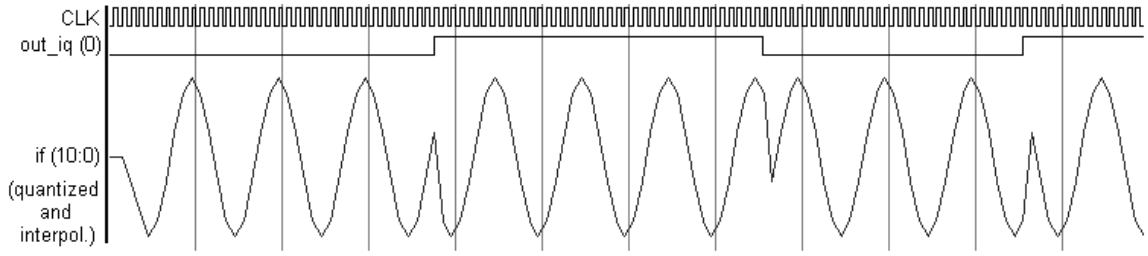

Fig. 4: Modelsim simulation of BPSK modulation (f_{clk}=100 MHz, f_c = 10 MHz).

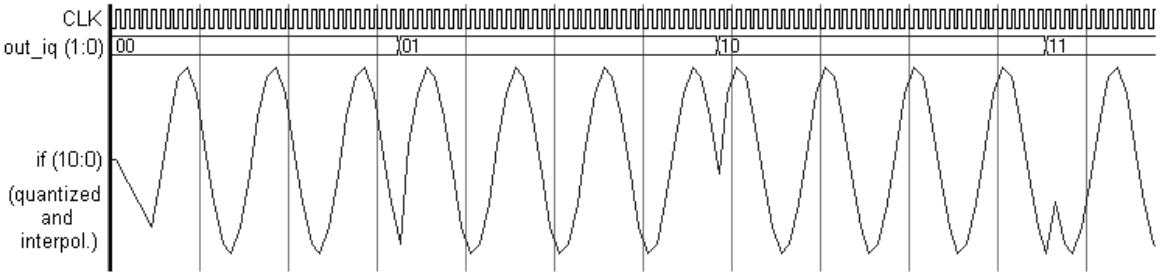

Fig. 5: Modelsim simulation of QPSK modulation (f_{clk}=100 MHz, f_c = 10 MHz).

3.3. MAPPING

After proper simulation the created model of modulator is now mapped to the FPGA. It was chosen the appropriate FPGA device Virtex II XC2V40 in accordance with use of system resources. Functional model has been mapped to the certain FPGA with these results:

Resources used for selected FPGA device Virtex II XC2V40:

Number of Slices:	60 out of 256	23%
Number of Slice Flip Flops:	98 out of 512	19%
Number of 4 input LUTs:	68 out of 512	13%
Number of BRAMs:	1 out of 4	25%

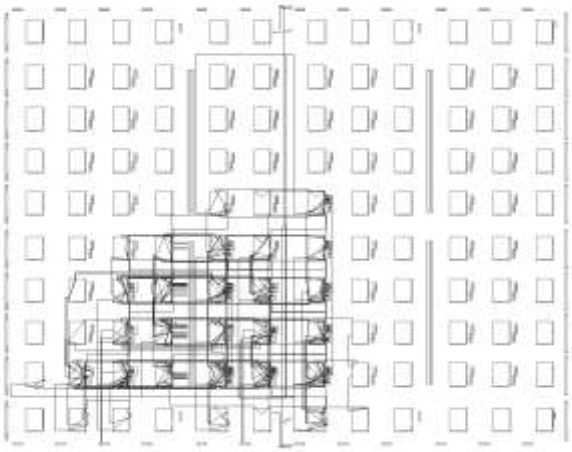

Fig. 6: Modulator floorplan in Virtex II XC2V40 FPGA device.

4. SUMMARY

The specific digital design from analysis over creating the simulation model to mapping the modulator to the FPGA was shown in this paper. The simplicity of construction was reached using intelectual property component in a combination with the VHDL language. Properly configured and wired components created functional model, which is showed in simulation diagrams. This model was finally mapped to a certain device.

The last step remained the configuration of this design to the physical FPGA structure. Further aim is to create the functional model of demodulator and to control its DSP components using the embedded processor.

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