REDUCTION OF STATIC POWER DISSIPATION IN SRAM

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ABSTRACT

The objective of this work is to investigate and propose methods to reduce static power dissipation for embedded SRAM, this investigation will mainly focus on 65 nm. The gain of every proposed method should be clearly defined. It is also important to keep in mind taken further system level impact, integration and implementation aspects.

1 INTRODUCTION

Embedded memory blocks have become dominant parts of integrated digital circuits and this trend still continues. In advanced CMOS technologies, the number of transistors on a chip increases, and static power dissipation is becoming a problem. In the standby mode memory block consumes, due to a leakage, see figure 1, an amount of energy which is increasing every technology step. This is caused by the scaling transistor's geometric dimensions.

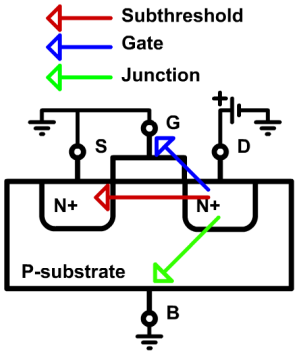

Figure 1: Leakage components in NMOS transistor.

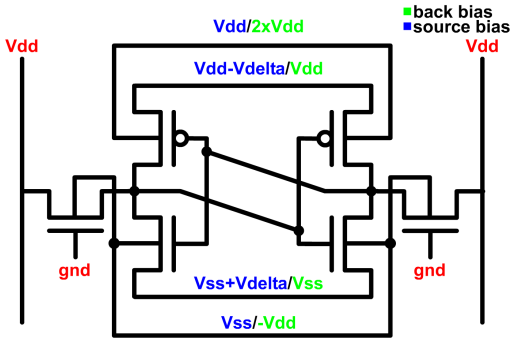

Figure 2: Voltage levels in 1 bit cell for back and source bias.

The possible methods, on how to reduce static power disipation in memories, will be studied, can be divided into two groups: with and without data retention. Into the first group belong these methods: voltage reduction (vr), back bias, source bias (sb) [1], split V_{dd} and into the second this one method: power off switch (POS).

Methods with data retention are methods where content of memory is kept and memory is put into standby mode. After "waking up" valid data can be read. POS method switch whole memory off this results in lost of the memory content. Is assumed that the memory is not in operation mode. Only snadby mode will be observed.
This report focuses on these data retention techniques except split V_{dd}.

2 CELL INVESTIGATION

For the SRAM memory cell manufacturing the transistors with high threshold voltage are used. For leakage reduction investigation standard 6-T bit cell, was used and different conditions according to investigation method were applied. See figure 2.

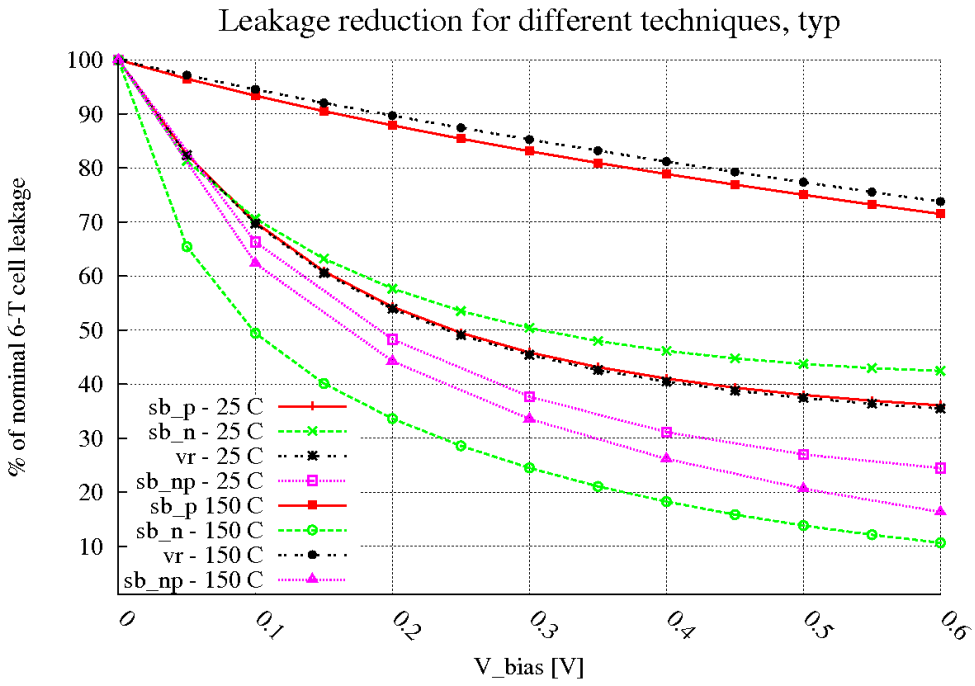

Figure 3: Leakage reduction dependency vs biasing condition

Figure 3 shows leakage reduction effectivity for different methods, temperatures and typical process corner. As can be seen the most effective leakage reduction method, is source biasing NMOS and PMOS transistors at the same time. Increasing the temperature has a bad influence on the subthreshold current. This results in a decreasing effectivity of voltage reduction and source bias PMOS transistors. Leakage currents flow through pass-gate, which has on drain and source terminals "V_{ss}" and "V_{dd}" respectively, and open pull-down transistor.
Back biasing is not ploted, because of transistors under back bias condition shows dramatic leakage current increas, due to junction current.

3 DATA RETENTION

There is no method how define sucure data retention voltage (DRV) level. For DRV level definition was used static noise margin (SNM) of not accessed cell. As a reference for conversion of the SNM value to the number of sigma was used value given by Crolles2 Alliance. For

DRV invesigation was taken the worst process corner at worst temperature. Number of sigma is calculated from yield and from guaranteed percentage of working cells.
However, in this stability investigation are not included stress conditions, like different noise sources and temperature changes. This can be only verified by silicon qualification.

4 IMPACT ON MEMORY

A simulation model of memory compilerwas made for impact investigation of leakage reduction methods on larger range. This model follows the configuration parameters of a real compiler. This model included all main leakage contributors and memory was divided into two parts: periphery and matrix.

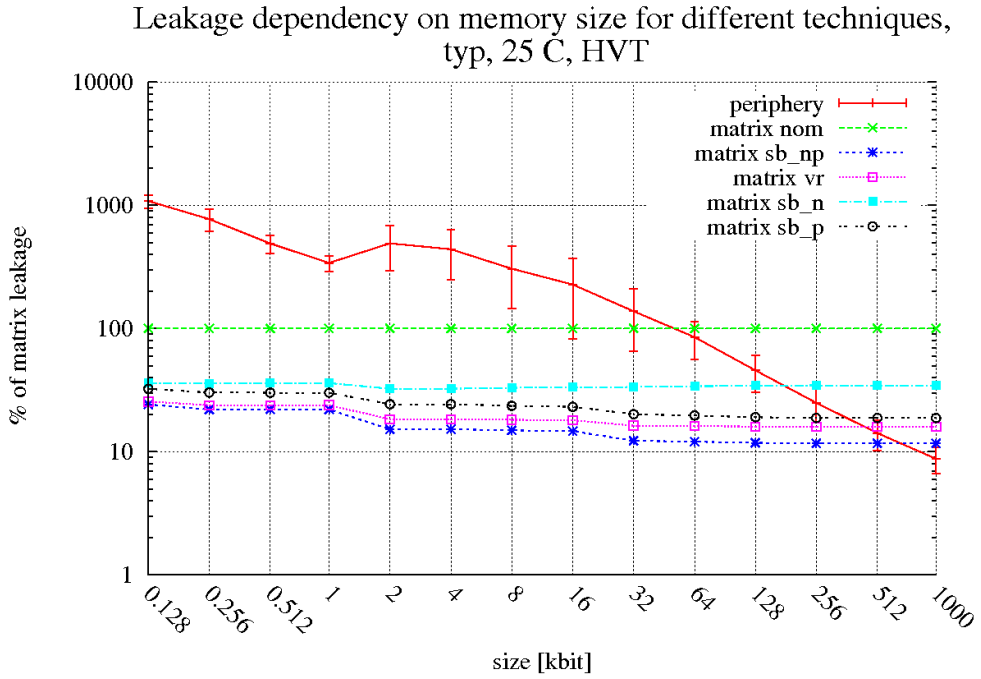

Figure 4: Leakage reduction over compiler range, using different techniques.

As shown in figure 4 we can clearly observe that the dominant leakage contributor for small instances is not the memory matrix but it is the periphery. According to these values it can be decided if applying these leakage reduction methods will save power and how much.

5 CONCLUSION

This report shows the possibility of different data retention methods and their impact on leakage in the memory.

REFERENCES

[1] Nii K. et al., A 90-nm Low-Power 32-kB Embedded SRAM With Gate Leakage Suppression Circuit for Mobile Applications, IEEE journal of Solid-State Circuits, vol. 39, No. 4., str 684-693, 2004