FORMAL MODEL OF TESTABLE BLOCK

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ABSTRACT

Formal model of a circuit on RT level is described in this paper. The model is used to describe properties of Testable Block. It is indicated how the concept of Testable Block can be used to reduce RT level test application time by decreasing the number of register included into scan chain.

1 INTRODUCTION

In this paper, the concept of Testable Block (TB) is defined. It is also indicated how TB can be used to increase testability parameters in terms of controllability and observability of internal nodes of CUA(Circuit Under Analysis).

TB can be seen as a segment of a digital circuit which is fully testable through its inputs and outputs – boundary registers or primary inputs/outputs of CUA. Such an approach can be used to reduce the number of registers included in scan chain. Border registers are the only registers which can be used as scan registers. In our methodology, TBs will be identified through evolution algorithm which will operate on a formal model of CUA. The purpose is to subdivide the circuit into number of TBs.

2 FORMAL MODEL OF CIRCUIT ON RT LEVEL – BASIC DEFINITIONS

This model was defined in [1], for the purposes of identification of TBs it had to be further extended. The basic quintuple describes the overall structure of circuit. It is based on basic elements of circuit on RT level such as element, port and connection.

The identification of TBs is based on definitions and rules, they will follow now together with the explanation of the reasons for them.

Definition 2.1:
Let *UUA=(E, P, C, PI, PO)* is ordered quintuple reflecting CUA structure model on RTL level. Then *E* is the set of circuit elements, *P* is the set of elements ports, *C* is the set of connection, *PI* is the set of primary inputs, *PO* is the set of primary outputs.

This definition is based on traditional view on digital circuit and describes circuit

structure using quintuple of sets. The methodology described in this paper is supposed to be used on RTL structure only, therefore elements which can appear in such a structure, must be clearly defined.

Definition 2.2:
Let $E=(R \cup MX \cup FU)$ be the set of circuit elements in RTL structure, where R is the set of registers, FU is the set of functional units, MX is the set of multiplexers.

This separation is important for testability analysis purposes. The set of the registers represents all elements with memory character which cause sequential behaviour of CUA. The elements from the MX set control the data flow and the elements from the FU set have a behaviour of combinational elements.

For the purposes of structural analysis it is also important to define the set of all ports as the points through which diagnostic information will be transported. Each element has ports through which it is connected to ports of other elements or primary inputs/outputs.

Definition 2.3:
Let $P=(IN \cup OUT \cup CI)$ be the set of all ports in an RTL structure, where IN is the set of input ports, OUT is the set of output ports, CI is the set of control and synchronizing ports.

Example 1:
The use of the previous definitions will be demonstrated now on multiplexer with two inputs and one output: $\{MX_1\} \subset E$, with two data inputs a and b, one output y and one address switch sel. Then $\{a, b, y, sel\} \subset P$ and $\{a,b\} \subset IN$, $\{y\} \subset OUT$, $\{sel\} \subset CI$.

For the purposes of developing the model, such mechanisms must be created which assign ports from P set to elements which exist in CUA (to registers, FUs and multiplexers).

Definition 2.4:
Let the function: $\psi: E \rightarrow 2^P$ be defined, which assigns elements from the set of ports to each circuit element, then:

1. $\psi(e) = \{p | p \text{ is the port of element } e\}$
2. The function ψ is defined for all elements of set E.
3. $e_1 \neq e_2 \Leftrightarrow \psi(e_1) \cap \psi(e_2) = \varnothing$.

Thus, the function ψ creates the link between the set of elements and the set of ports and assigns the set of ports to elements. The condition 2) provides that the set of ports can be identified for each element. Condition 3 tells that each port belongs to one element only.

All the elements in CUA are interconnected through the connections. The concept of connection is covered by the following definition.

Definition 2.5:
Let C be the set of connections, then $C \subset (PI \cup P) \times (PO \cup P)$.

The set of connections is a binary relation on the set of ports, the set of primary inputs and the set of primary outputs. The set of connections is the union of topples of ports between which a connection exists. It can be stated that C is reflective, symmetric and transitive. Proof is given in [1].

3 TESTABLE BLOCK

The model of TB will be developed in this chapter. A Testable Block is a segment in

CUA separated by registers from other segments. It is guaranteed that the circuitry of TB is testable through its inputs and outputs, transparency properties of CUA are utilized to apply the test. As the consequence, the number of registers included into scan chain is decreased.

A TB must fulfill the following features (the features are supported by formal definitions and rules):

Feature 1: A TB is a segment of CUA.

It is easy to imagine that if E_{TB} is the set of elements of TB, then it is also a subset of E set, P_{TB} is the set of ports of elements from the set E_{TB} and subset of P, C_{TB} is the set of connections in TB and subset of C. Thus, the structure of a TB can be defined according to the next definition.

Definition 3.1:
Let TB=(E_{TB}, P_{TB}, C_{TB}, PI_{TB}, PO_{TB}) is ordered quintuple which reflects the structure of Testable Block, then $E_{TB} \subseteq E$, $P_{TB} \subseteq P$, $C_{TB} \subset ((PI_{TB} \cup PO_{TB} \cup P_{TB}) \times P) \cup (P \times (PI_{TB} \cup PO_{TB} \cup P_{TB}))$, $PI_{TB} \subseteq PI$, $PO_{TB} \subseteq PO$.
The set C_{TB} contains also the connections from and to TB, not only connections inside TB.

Feature 2: A TB is separated from other TBs by registers.

The TB separation from other TBs by registers means that the registers in the border create an interface for applying the test to elements inside the TB.

Every connection from the port of an element inside TB which does not start or does not end in the register inside TB must end or start in the element inside TB or on primary input or primary output. This is to say that FUs and MXs inside TB must not have their ports connected to ports outside TB, the connection is possible through registers only. This condition is reflected by the following definition. Feature 2 is supported by the following two definitions.

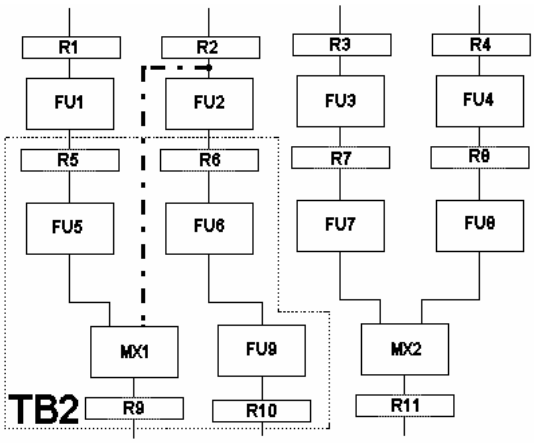

Fig. 1: *example of Testable Block TB2 separated by registers R5, R6, R9, R10 (border registers) and shows not allowed dash dotted connection*

Definition 3.2:

$$\forall (p_1, p_2) \in C_{TB} \text{ where } p_1 \in P_{TB} \wedge p_1 \notin \bigcup_{r_i \in R_{TB}} \psi(r_i) : p_2 \in (PO \cup PI \cup P_{TB})$$

Definition 3.3 (symmetric to 3.2):

$$\forall (p_1, p_2) \in C_{TB} \text{ where } p_2 \in P_{TB} \wedge p_2 \notin \bigcup_{r_i \in R_{TB}} \psi(r_i) : p_1 \in (PO \cup PI \cup P_{TB})$$

$\bigcup_{r_i \in R_{TB}} \psi(r_i)$ is the set of all ports of the registers from TB.

A test to a digital synchronous circuit is applied through registers. The identification of the registers is the goal of testability analysis methodologies, our methodology is based on the identification of **border registers.**

Feature 3: TBs are separated from each other by registers.

The definition of the border registers is used later to simplify other definitions.

Let $\boldsymbol{BR \subseteq R_{TB}}$ be the set of registers which has at least one connection to the outside of TB.

Definition 3.4 (set of border registers):
Let $\boldsymbol{BR \subseteq R_{TB}}$ and $\forall r \in BR : \exists p \in \psi(r) \wedge \exists (p_1, p_2) \in C_{TB}$ then $p_1 = p \wedge p_2 \in (P \setminus P_{TB})$ or $p_1 \in (P \setminus P_{TB}) \wedge p_2 = p$

For each register *r* from *BR*, *p* port exists from the set of the ports of the register r and pair p_1, p_2 exist from the set of connections of TB then p_1 must be from the set of ports of the register r and p_2 must be a port which is not from the TB or symmetric p_2 but must be from the set of ports of the register r and p_1 must be a port which is not from the TB.

Feature 4: All egisters which are inside a TB must not be included into scan chain.

Rule 1: $(R_{TB} \setminus BR) \not\subset SCAN$

As the consequence, the number registers included into scan chain is decreased.

Feature 5: All elements $(MX_{TB} \cup FU_{TB})$ in TB must be testable through inputs and outputs of TB (through border registers), transparency properties of CUA are utilized to apply the test.

Rule 2: $\forall e \in (MX_{TB} \cup FU_{TB})$: all elements *e* must be controllable/observable from/on primary inputs or from/on *BR*.

Feature 6: Any TB must not overlap another TB (any two TBs must be disjunctive).

The reason for this statement is such that the goal of the testability analysis methodology is to apply the test of any two TBs in parallel.

Rule 3: Let for each TB1 and TB2, where TB1≠TB2, then it must hold:

- FU_1 and FU_2 are disjunctive sets
- MX_1 and MX_2 are disjunctive sets
- $(R_1 \setminus BR_1)$ and $(R_2 \setminus BR_2)$ are disjunctive sets

Rule 4: Border registers can be shared between two TBs.

4 CONCLUSIONS AND PERSPECTIVES FOR THE FUTURE RESEARCH

In this paper, the concept of Testable Block developed on formal model of a circuit on RT level was presented. The concept of TB will be further developed to reduce RT level test application time by decreasing the number of register included into scan chain.

In the forthcoming period the model will be possibly extended if it appears that it is necessary for the purposes of testability analysis. Our intention is as follows:

1. Methodology based on the usage of optimization algorithms (genetic algorithms, simulated annealing) will be created.
2. The methodology will be implemented on the formal model.
3. Testability analysis algorithms operating on the formal model will be developed.

We expect that it will be clearly demonstrated that:

1. Testability analysis utilizing the concept of TB can be performed on a formal model based on concepts of discrete mathematics and theory of graphs.

2. The problem of testability analysis based on the concept of TB can be converted into problems whose solutions are well known in discrete mathematics and theory of graphs.
3. Optimization algorithms can operate on formal models and utilize all the concepts offered by this discipline, currently quite widely utilized.
4. The concept of TB can increase testability parameters of digital components.

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REFERENCES

[1] Růžička, R.: Formální přístup k analýze testovatelnosti číslicových obvodů na úrovni RT (disertační práce), FIT VUT v Brně, 2002, 110 pp.

[2] Kotásek, Z.: Uplatnění principů řiditelnosti/pozorovatelnosti při návrhu číslicových obvodů (habilitační práce). FEI VUT v Brně, 1999, 80 pp.

[3] Crouch, Alfred L.: Design-for-test digital IC’s and embedded core systems. Prentice Hall PTR, ISBN 0-13-084827-1, 1999, 349 pp.

[4] Hlavička, J.: Diagnostika a spolehlivost číslicových systémů. ČVUT Praha, 1978, 197 pp.

[5] Pečenka, T.: Metodika analýzy testovatelnosti obvodu na úrovni RT (diplomová práce). FIT VUT v Brně, 2003, 57 pp.

[6] Chakradhar S. T., Agrawal V. D., Bushnell M.L.: Neural Models and Algorithms for Digital Testing. Kluwer Academic Publishers, 1991, ISBN 0-7923-9165-9, 184 pp.

[7] Kotásek Z., Strnadel J., Pečenka T.: Methodology of Selecting Scan-Based Testability Improving Technique, In: Proc. of 8th IEEE Design and Diagnostic of Electronic Circuits and Systems Workshop, Sopron, HU, UWH, 2005, p. 186-189, ISBN 963-9364-48-7

[8] Kotásek Z., Pečenka T., Strnadel J.: Improving Testability Parameters of Pipelined Circuits Through the Identification of Testable Cores, In: Proc. of the 7th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems, Bratislava, SK, SAV, 2004, p. 99-104, ISBN 80-969117-9-1

[9] Kotásek Z., Růžička R.: Behavioral Analysis for Testability on VHDL Source File, In: Proceedings of Design and Diagnostics of Electronic Circuits and Systems Workshop, konference IEEE DDECS, Bratislava, SK, SAV, 2000, p. 209-212, ISBN 80-968320-3

[10] Kotásek Z., Růžička R.: Testability Analysis Based on Discrete Mathematics Concepts, In: Proc. of the 9-th International Colloquium on Numerical Analysis and Computer Science with Applications, Plovdiv, BG, 2000, p. 113

[11] Růžička R.: The Formal Approach to the RTL Test Application Problem Using Petri Nets, In: Proceedings of IEEE Design and Diagnostics of Electronic Circuits and Systems 2002, Brno, CZ, FIT VUT, 2002, p. 78-86, ISBN 80-214-2094-4

[12] Hlavička J., Kotásek Z., Růžička R.: Formal Approach to RTL Testability Analysis, In: IEEE LATW 2000, Rio de Janeiro, BR, 2000, p. 98-103