PHASE-LOCKED LOCAL OSCILLATOR FOR A K-BAND DOWNCONVERTER

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ABSTRACT

This paper deals with design and realization of a microwave phase-locked oscillator (PLO) which is intended for use as a local oscillator in a K-band downconverter. Design goal was to achieve very low phase noise and spurious free signal with a sufficient power level at the output frequency 11.952 GHz. For that purpose a low phase noise MMIC VCO was used in phase locked loop. The PLL works at half the output frequency, therefore there is a frequency doubler at the output of the PLL. Output signal from the frequency doubler is filtered by a bandpass filter and finally amplified by a single stage amplifier.

1 INTRODUCTION

Local oscillator (LO) signal directly affects the properties of intermediate frequency (IF) signal and consequently the quality of the received information. If the LO signal had some spurious spectral components, it may cause conversion of unwanted signals to IF. Also, phase noise of the LO causes distortion of the converted signal, especially in the case of phase modulation. Therefore, it is important to achieve low phase noise, and spurious free signal of the local oscillator.

The best results can be obtained with a dielectric resonator oscillator [1], especially if it is phase-locked. However, components for dielectric resonator oscillator design are not commonly available. Therefore, I decided to design a low cost solution using commercially available integrated circuits.

2 CONCEPTION AND DESIGN OF THE PLL SYNTHESIZER

Block structure of whole PLO is shown in Fig. 1. A VCO running at half the desired output frequency was available. Therefore, the PLL works at 5.976 GHz and its frequency is multiplied by two to achieve 11.952 GHz. Unfortunately this compromise brings in phase noise degradation of the output signal by 6 dB compared to the PLL signal.

The phase locked loop is designed using monolithic microwave integrated circuits produced by Hittite Microwave Corporation. The HMC431 voltage controlled oscillator

running on frequency 5.976 GHz is phase locked to a reference signal at 119.52 MHz. The reference signal is generated by the 5th overtone quartz oscillator. This promises low phase noise close to the carrier. Signals from the reference oscillator and feedback loop come to inputs of the digital phase-frequency detector (PFD) HMC439. The PFD is intended for use in low noise PLL applications because of its ultra low phase noise floor. Output signal of the PFD is filtered by active loop filter utilizing fast and low noise operational amplifier THS4031. The VCO delivers about 2 dBm of output power to a microstrip directional coupler. The coupled signal is used as feedback and it is divided by a divider chain with a total division ratio of 50. This results in frequency 119.52 MHz according to the reference signal. Two divide-by-5 HMC438 and one divide-by-2 HMC364 low noise dividers are used.

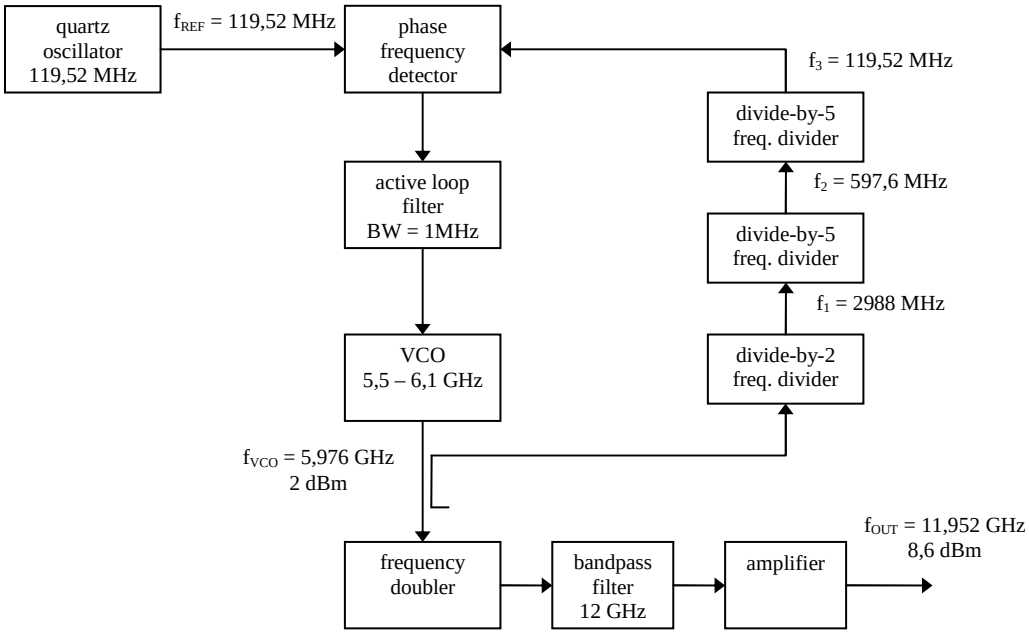

Fig. 1: *Block structure of the phase-locked local oscillator.*

2.1 THE LOOP FILTER DESIGN

Outside the loop bandwidth, the noise of the free-running VCO is the dominant noise contributor. VCO phase noise is suppressed inside the loop bandwidth. According to [2] the loop filter bandwidth was designed to be 1 MHz. This should ensure minimal phase noise of the PLL. The damping factor ξ is a measure of stability of the PLL and it influences the settling time of the loop. In the case of this local oscillator, there is no need of a short settling time. Therefore the damping factor was chosen to be ξ=1, to avoid stability problems. Fig. 2 shows an active loop filter with an op-amp used in the synthesizer. *PD D OUT* and *PD U OUT* are differential outputs of the phase detector. More detailed information about the design can be found in [3].

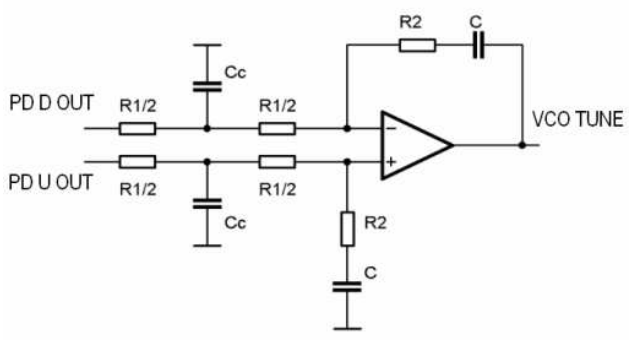

Fig. 2: *Active loop filter.*

2.2 DIRECTIONAL COUPLER, FREQUENCY DOUBLER, BANDPASS FILTER AND AMPLIFIER DESIGN

The directional coupler consists of quarter wavelength microstrip coupled lines. Coupling loss is approximately 12 dB which ensures an excitation power of about -10 dBm at the input of the frequency divider. The unused gate is terminated using a characteristic impedance and RF ground. An active frequency doubler utilizing one MGF1302 GaAs FET was designed to multiply the PLL frequency by 2. The frequency doubler simulated conversion gain is about 0.3 dB. To obtain clear output spectrum, the resulting signal is filtered by a bandpass filter. The filter consists of two coupled half−wave resonators and its insertion loss is only 0.6 dB at the center frequency of 11.952 GHz. The filtered signal is amplified by a single stage amplifier. The amplifier is designed using MGF1303 with a simulated gain of 8.4 dB. The total conversion gain of the frequency doubler, bandpass filter and amplifier is 7.9 dB. The simulated output power of the PLL synthesizer is almost 10 dBm. More detailed information about the design can be found in [3].

Fig. 3 shows a photograph of the PLO without the reference quartz oscillator. The reference oscillator is attached to the PLL synthesizer via the SMA connector. The PCB material is the microwave substrate DiClad 870 with gold metallization.

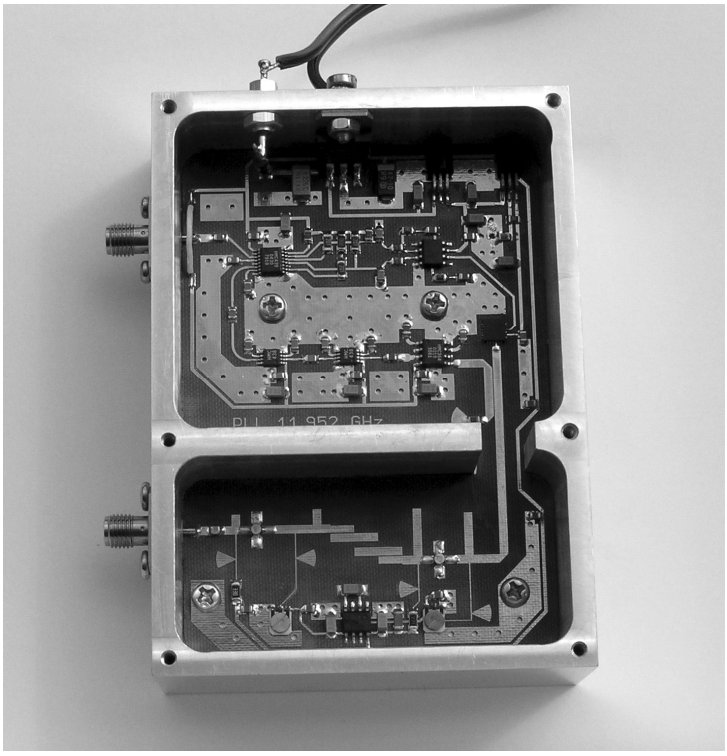

Fig. 3: *11.952 GHz PLL synthesizer.*

3 MEASURED RESULTS

Overall phase noise of the PLO was predicted in terms of the loop filter bandwidth, phase noise floor of the frequency dividers and free running VCO phase noise. The dashed line in Fig. 4 shows the estimated phase noise of the PLL synthesizer. Suitable phase noise measurement method wasn't available, therefore the phase noise performance wasn't verified.

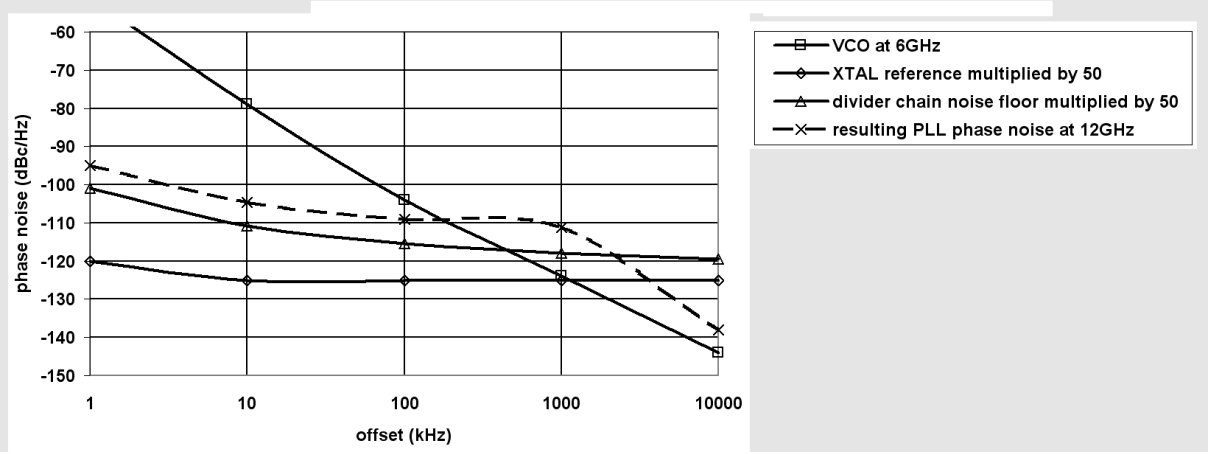

Fig. 4: *Estimated phase noise of the phase-locked oscillator.*

Fig. 5 shows the spectrum of the output signal measured using HP E7404A spectrum analyzer. We can see, that the spectrum is without any spurious components. Power level of the carrier is 8.6 dBm, which is only 1.4 dB less than the simulated value.

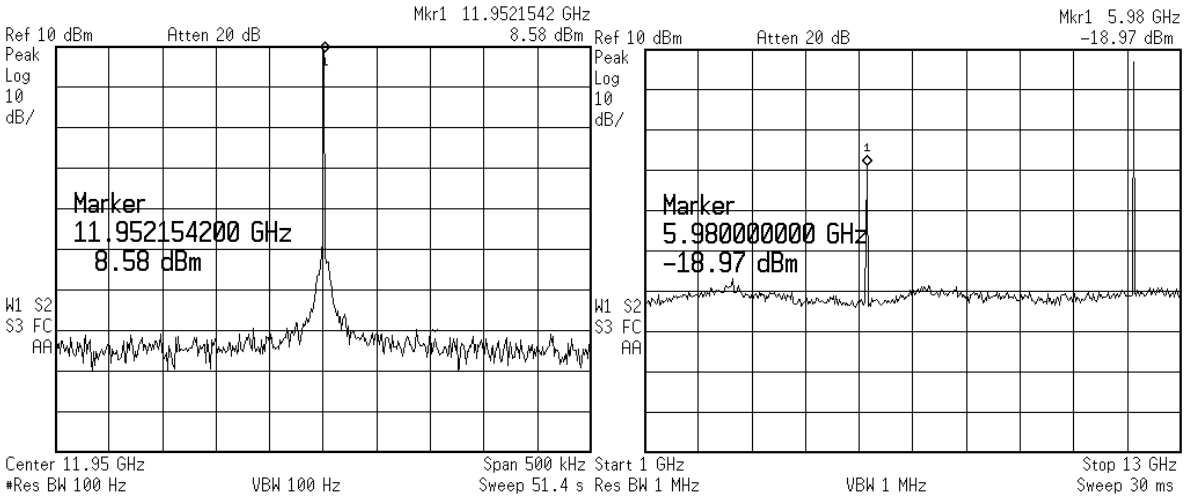

Fig. 5: *Measured spectrum of the output signal.*

It is obvious that there is only one undesirable signal at a frequency of 5.976 GHz. It is the fundamental frequency of the VCO, suppressed by 28 dB compared to PLL synthesizer's first harmonic. There are no more spurious spectral components in wide bandwidth so we can say that the spectral purity is much better than in the case of a signal source realized by means of multiplying a quartz oscillator. Tab. 1 shows main characteristics of the PLO.

Output frequency	11.952	GHz
Output power	8.6	dBm
Estimated phase noise f_{offset} = 1 kHz	-95	dBc/Hz
f_{offset} = 10 kHz	-105	
Reference signal frequency	119.52	MHz
Supply voltage	+12	V
Supply current	510	mA

Tab. 1: *Phase-locked oscillator - main characteristics.*

4 CONCLUSION

In this paper design and realization of the phase-locked local oscillator for the K−band downconverter is presented. The PLO consists of two parts – the PLL synthesizer and the reference quartz oscillator. Output frequency of the PLL synthesizer is 11.952 GHz with a power level of approximately 8.6 dBm. Estimated phase noise is -95 dBc/Hz at offset frequency of 1 kHz. The output signal spectrum is clean and there are no spurious signals close to the first harmonic. The PLL synthesizer meets the design requirements and it can be used as a low-phase-noise local oscillator.

ACKNOWLEDGEMENTS

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