FPGA IMPLEMENTATION OF AN SDDR CORE FOR RADIO TRANSCEIVER

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ABSTRACT

Today's technology and efficiency of the hardware components intended for the digital signal processing offer a great potential to revolutionize the way how radio transceivers are designed. The potential to create the IF sampled software defined digital radio *(SDDR)* cores for the traditional analog systems, as well as for the modern digital communication transceivers utilizing digital techniques of modulation, algorithms of the adaptation, synchronization, and decoding, completely in the digital domain. This work offers a prototype of such SDDR core for the radio–data modem implemented mainly in an FPGA. The design itself was preceded by a complete simulation in MATLAB–Simulink.

1 INTRODUCTION

The modern approach of the SDDR core design comes with an ambition to digitize an incoming signal as closest to the antenna as possible and thus to increase flexibility of the design and to bring the advantages of the digital signal processing to main parts of the radio transceiver. However, it should be done with respect to the overall dynamic performance of the whole solution. The new factors which limit the dynamic range such as a maximum achievable SNR performance of the ADC (1), aperture uncertainty and construction of the anti-aliasing filters must be taken into consideration when choosing of the frequency plan of the SDDR core and designing its main parts.

2 QUANTIZATION NOISE AND APPERTURE UNCERTAINTY

Besides the advantages, the digitalization of the received signal introduces another source of distortion in radio technique – *the quantization noise*. The SNR performance of the N-bit ADC converter can be found according to (1).

$$SNR_{ADC} = 6.02.N + 1.76[dB] \ , \ Noise\ Bandwidth = 1.\ Nyquist's\ zone \qquad (1)$$

The dynamic range of the ADC is mostly limited by the quantization noise and thus by the number of bits, but it can be easily degraded (2) by not carefully designed clock circuitry.

Following calculation shows how challenging and rather difficult is to design proper clock circuitry with increasing the intermediate frequency *(IF)* of the SDDR core – without significant ADC performance degradation:

$$SNR_{\deg raded} = -20.\log\left(2.\pi.f_{ana\log}.t_{j\_rms}\right) \qquad (2)$$

Assuming the incoming IF signal with a frequency of 71 MHz and a 12–bit ADC converter (ADS5520 chosen), the spectral purity of the clock signal can be calculated as follows:

- 12-bit ADC converter ADS5520: $SNR_{ADC,FS} = 68dB, @70MHz, S = -1dBFS$ (3)
- $SNR_{\deg raded}$ at least 6dB higher not to degrade the overall SNR performance more than 1dB: $SNR_{\deg raded} = 74dB$ (4)
- Resultant clock jitter t_{J_rms} from (1): $t_{J\_rms} = \dfrac{\sqrt{10^{-\frac{SNR_{\deg raded}}{10}}}}{2.\pi.f_{ana\log}} = \underline{0.45ps}$ (5)
- And finally the average noise power spectral density caused only by the timing jitter of the clock signal within the 1.Nyquist's zone assuming $f_{clk} = 19.2MHz$ and a full scale signal level of 12dBm.

$$PSD_{phase\_noise} = S_{FS}[dBm] - SNR_{\deg raded}[dB] - B_{NyguistZone}[dBHz]$$
$$PSD_{phase\_noise} = 12dBm - 74dB - 10.\log\left(\frac{19.2MHz}{2}\right)dBHz = \underline{-132dBm/Hz} \qquad (6)$$

3 FREQUENCY PLAN OF THE DIGITAL RECEIVER

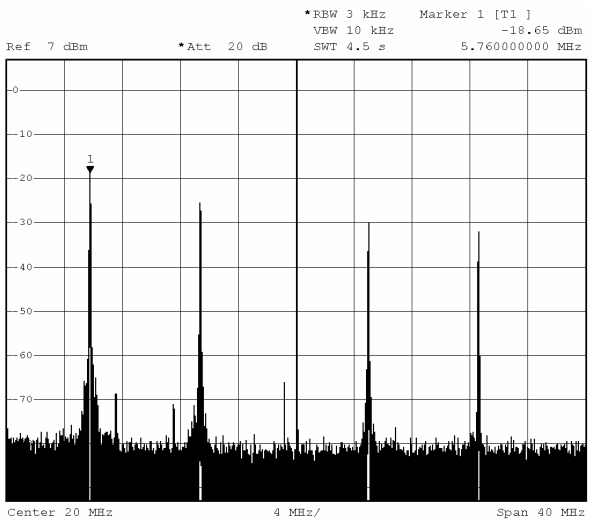

Fig. 1: *Depiction of the first four Nyquist's zones with a real narrow bandwidth signal after undersampling. GMSK R_b=98kbps, BT=0.5.*

Although, a maximum sampling frequency of the ADC is 125 MSPS, it is not necessary, moreover highly inefficient to choose the sampling frequency for which the sampling theorem for the IF carrier frequency is fulfilled. Instead, a phenomenon called undersampling or harmonic sampling is used. The *figure 1* shows a frequency spectrum of the input IF signal with a frequency of 71 MHz after undersampling. The sampling frequency chosen for SDDR core is 19.2 MHz, which results the input IF carrier signal to be undersampled by a factor of 8. The undersampling represents the first part of the digital down conversion block and translates the IF input signal to the frequency of 5.8 MHz – the desired signal for further processing is aliased to the first Nyquist's zone. The sampling theorem for such bandwidth limited signal is fulfilled as can also be seen in *figure 1*.

4 FPGA IMPLEMENTATION OF THE DIGITAL CORE

The software defined digital core *(fig. 2)* is implemented in an FPGA–Cyclone II circuit manufactured by Altera Corp. The 12-bit data words are passed synchronously from the ADC into the frequency translator which consists of complex Numerically Controlled Oscillator *(NCO)* running at the frequency of 5.8MHz and two 12-bit multipliers. The signal is down converted to the zero frequency and thus contains a *quadrature Q* and an *in-phase I* component. Both components are further processed – decimated by the 4-stage CIC filters with decimating factor of 10; time–multiplexed together; this double data rate signal is filtered by a main channel selectivity FIR filter of the 70th order, which is running at the

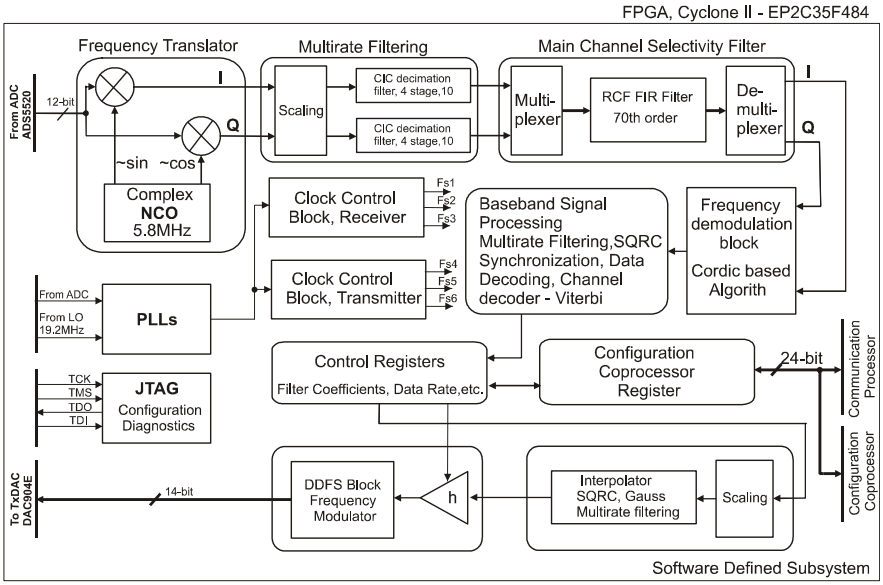

Fig. 2: *Simplified block diagram of the SDDR core implemented in an FPGA.*

double processing speed; de–multiplexed and both I, Q components are than passed into the frequency demodulator. Up to this point the algorithms have been designed and the robustness of the solution has been successfully tested by replacing the equivalent analog parts of the radio receiver and by a follow–up BER evaluation. Future work will include the design of a baseband signal processing block – synchronization and the data decoding block, according to the modulation format chosen – and an upconverter blocks which are essential for digital communication.

5 CONCLUSION

The main advantages of the suggested solution hopefully are a greater flexibility, possibility to use various digital modulation techniques with a constant modulation envelope such as GMSK, 2–CPFSK, 4–CPFSK, configurable channel bandwidth, modulation rates and prospective digital signal processing algorithms for synchronization and decoding.

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