TECHNIQUES FOR CHARACTERIZATION OF INTEGRATED NONLINEAR CAPACITORS

Ing. Tomáš SUTORÝ, Doctoral Degree Programme (2)
Dept. of Radio Electronics, FEEC, BUT
E-mail: xsutor00@stud.feec.vutbr.cz

Supervised by: Dr. Zdeněk Kolka

ABSTRACT

The paper deals with techniques for capacitance characterization of integrated nonlinear capacitors on a chip. Several methods are compared, main part is about CBCM method (Charge-Based Capacitance Measurements) and it's application to the nonlinear capacitance characterization. Since its invention the CBCM method has been extensively used for on-chip interconnect linear capacitance measurements. However, it can be also used for nonlinear device characterization. Application of CBCM to CMOS gate-capacitance measurements is presented.

1 INTRODUCTION

When designing analog integrated circuits, we are interested, beyond other parameters, in capacitance of capacitors and diverse parasitic capacitances for example nonlinear MOS gate-capacitance. With increasing working frequency and density of integration these requirements are more important. Measurements of real devices must be done to determine technological constants and to create models of devices, mainly capacitors, but also for modeling parasitic behavioral of other devices. Conventional methods suitable for standard discrete devices are not useful for this purpose. The resolution is very poor to reach a satisfactory result. Fortunately there exist some methods, which are capable to measure, and this paper describes these.

2 METHODS

There are several methods for measurements of nonlinear on-chip capacitances in the femtofarad range. They differ in principles, in demands on measuring instruments, and in accuracy and resolution.

2.1 PARALLEL CONNECTION

The first very simple method is based on parallel connection of very high number of identical devices together. In such a way a big structure is created which will get the total

capacitance to an operating range of sensitive RLC meter. That structure takes large area on a chip and we must use the same structure but without devices for eliminating capacitance of connecting net and by this we calibrate the measurement. The result of measurement is average value of all samples in array. That does not enable to use this method for finding out distribution of measured parameters.

2.2 ON-CHIP SENSOR WITH REFERENCE CAPACITOR

Next method allows to measure capacitance in real range, but it is necessary to use known reference capacitor *C*. It is described in references [1]. Principle is shown in figure 1.

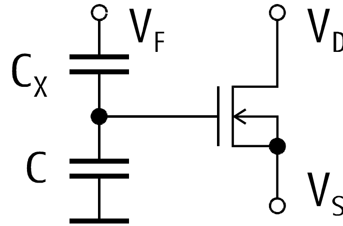

Fig. 1: *Test structure with capacitance divider and source follower*

There are capacitive divider and source follower in test structure. Transistor is working in saturation region as consequence of driving by constant current source. This ensures constant voltage V_{GS} and we can watch voltage on a transistor gate on V_S terminal with DC offset. If V_F is voltage with a known slope and we measure the output slope of V_S, we are able to determine unknown capacitance and its dependency of voltage:

$$C_X = C \cdot \frac{S}{1-S} \qquad (1)$$

where

$$S = \frac{C_X}{C + C_X} = \frac{dV_S}{dV_f} \qquad (2)$$

This method is limited by the size of parasitic capacitances of the sensor transistor. They should be negligible in comparison with measured and reference capacitance.

2.3 CHARGE METHOD

This method is described in references [2]. A small amplitude square wave signal $V_g(t)$ is applied across a measured capacitor at DC bias level V_G, see figure 2. The current is integrated, with the DC component being eliminated using a feedback leakage compensation circuit. The output of the circuit, V_0 is thus a transient charge waveform, $Q(t)$ generated by the applied small signal. The amplitude of the response waveform is proportional to the device capacitance, that is

$$C(V) = \frac{Q_{\max}(V)}{V_g} \qquad (3)$$

where V_g is the amplitude of the excitation square wave, and $Q_{max}(V)$ is the maximum value of the transient charge response curve. In this circuit is necessary to use Leakage

compensation circuit with regulating a DC voltage on the output.

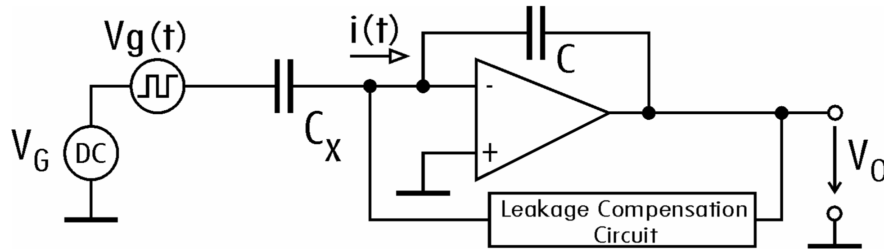

Fig. 2: *Principle of charge method*

2.4 CLASSICAL CBCM METHOD

The CBCM method (Charge-Based Capacitance Measurements) introduced in [3] has very good resolution that allows a measurement of capacitance in the femtofarad range. CBCM was originally developed for linear interconnect measurements. It is presented to explain principle of method that is described in chapter 2.5.

It does not need a reference on-chip capacitor. The only equipment needed for the CBCM method is an accurate amperemeter for the measurement of a DC supply current. Figure 3 shows the principle of classical version of CBCM.

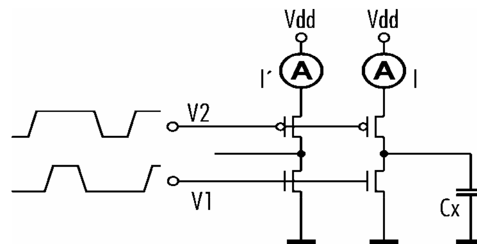

Fig. 3: *Classical version of CBCM method*

The test structure consists of a pair of NMOS and PMOS transistors connected in a "pseudo" inverter configuration, each has its own gate input. The pseudo inverter structure on the left is identical to the one on the right in every manner except that it does not include the target capacitance to be characterized. The left and right structures are both driven by two non-overlapping clock signals. When the PMOS transistor turns on, it will draw charge from *Vdd* to charge up the target measured capacitance. This amount of charge will then be subsequently discharged through the NMOS transistor into ground. An amperemeter measure this charging current. The difference between the two DC average current values is used to extract the target measurement capacitance *Cx* as given by

$$I - I' = C_x \cdot V_{dd} \cdot f \qquad (4)$$

where f is switching frequency and I and I' are introduced in figure 3.

The resolution limit of the method resides mainly in the mismatch of the drain junction and overlap capacitances between the left and right test structures in figure 3.

2.5 MODIFIED CBCM METHOD

The proposed modification of CBCM method is applicable to measurements of floating

devices. Two DC sources are used to measure the whole nonlinear characteristic in both polarities without necessity to switch the device under test (*Cx*). One source is swept while the other is kept constant and vice versa. For each point of the characteristic minimal voltage amplitude and thereby minimum DC current is guaranteed. Principal schematic of the proposed test structure is shown in figure 4.

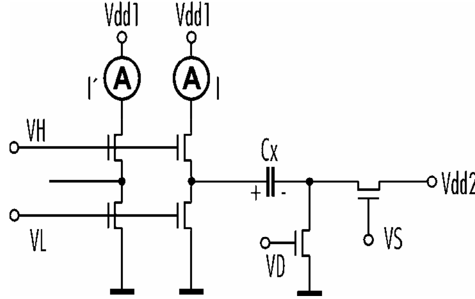

Fig. 4: *Modified CBCM method.*

The basic principle of CBCM with the main (right) and compensation (left) switches as shown in figure 3 is the same also for the modified method. The DC source *Vdd* was renamed as *Vdd1*. The main difference is on the negative terminal of the measured object. The ground connection is replaced by a switch and the node can be additionally connected to another DC regulated source *Vdd2* by a switch.

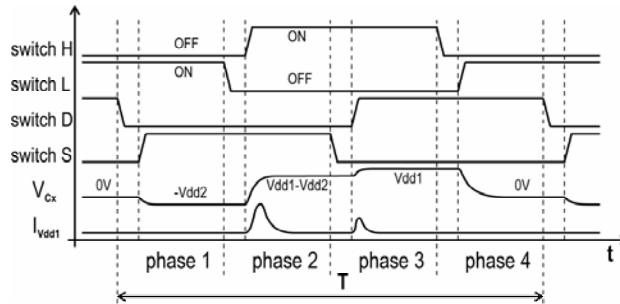

Fig. 5: *Waveforms of signals in modified CBCM method.*

During the phase 1 the measured capacitor is charged to negative voltage (seen on its terminals) from source *Vdd2* through switches L and S. During the phase 2 L is switched off and S is still switched on. Activation of switch H in the phase 3 causes charging the capacitor to voltage *Vdd1-Vdd2*. The charge drawn during 2→3 transient is counted by the amperemeter. The voltage changes for *Vdd1*. During the last phase S is switched off and the capacitor is charged to *Vdd1* through the switch D. The voltage changes for *Vdd2* and the charge drawn is again counted by the amperemeter.

The capacitor voltage varies during one period from *Vdd2* to *Vdd1* and the charge variation can be determined from the measured current as

$$\Delta Q(V_{dd2}, V_{dd1}) = \frac{I - I'}{f} = \int_{-Vdd2}^{Vdd1} C(v)dv \qquad (5)$$

The dynamic capacitance *C(v)* can be determined from reconstructed *Q-v* characteristic of the capacitor. Formula (5) gives only value of the charge variance.

Let me start the reconstruction of *Q-v* characteristic for negative voltages from *Vdd2* =

0. The voltage variation is then *Vdd1* and charge variation *ΔQ(0,Vdd1)*. For zero voltage the charge must be zero too, i.e. *Q(0) = 0*. This gives a fixed point in the characteristic. The change of charge due to sweeping of *Vdd2* is considered relative to this point. Finally we obtain

$$Q(-V_{dd2})_{Vdd1=const} = \Delta Q(0, V_{dd1}) - \Delta Q(V_{dd2}, V_{dd1}) \quad (6)$$

and similarly for the positive voltage

$$Q(V_{dd1})_{Vdd2=const} = \Delta Q(V_{dd2}, V_{dd1}) - \Delta Q(V_{dd2}, 0) \quad (7)$$

Thus the device can be characterized in both polarities by means of sweeping one source while the other is kept constant, figure 6. Both static and dynamic capacitances can be determined from *Q(v)*.

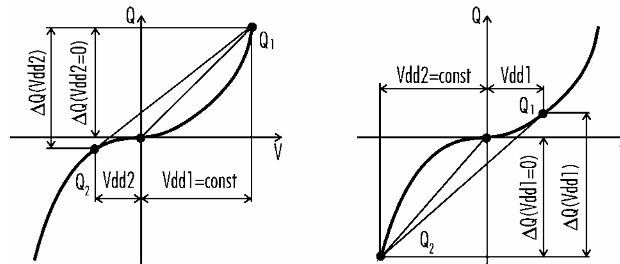

Fig. 6: *Both polarity reconstruction of Q-V characteristic.*

CONCLUSION

The overview of methods for small capacitance measurement was presented. A modification of CBCM for nonlinear capacitance characterization was proposed. Two DC sources are used to measure the whole nonlinear characteristic in both polarities without necessity to switch the measured object.

ACKNOWLEDGEMENTS

The paper has been prepared as a part of the solution supported by the Grant Agency of Czech Republic under the contract No. 102/03/H105.

REFERENCES

[1] Kortekaas, C.: On-chip Quasi-static Floating-gate Capacitance Measurement Method, Proc. of the IEEE International Conference on Microelectronic Test Structures, Vol 3, March 1990, pp. 109-113.

[2] Song, H., Dons, E., Sun, X. Q., Farmer, K. R.: Leakage Compensated Charge Method for Determining Static C-V Characteristics of Ultra-thin MOS Capacitors, Proc. of the NIST International Conference on Characterization and Metrology for ULSI Technology, 1998, pp. 231-234

[3] Chen, J. C., McGaughy, B. W., Sylvester, D., Hu, C.: An on-chip attofarad interconnect charge-based capacitance measurement (CBCM) technique, Proc. of IEDM'96, 1996, pp. 69-72