

FOLDED-CASCODE BULK-DRIVEN OTA

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ABSTRACT

The most significant problem to design the low-voltage operational amplifier is the limitation of the threshold voltage of the MOSFETs. In this paper an alternative new technique of Voltage Driven-Bulk CMOS, will be used to remove the threshold voltage requirement of MOSFETs from the signal path, and a device which is similar to the JFET transistor with depletion characteristics is obtained.

1 INTRODUCTION

An important factor concerning analog circuits is that the threshold voltages of future standard CMOS technologies are not expected to decrease much below what is available today. To overcome the threshold voltage a bulk-driven MOSFET has been used, it is well known that a reverse bias on the well-source junction will cause the threshold voltage to increase. Similarly, a forward bias on this junction will cause the threshold voltage to decrease. The bulk-driven transistor is a good solution to overcome the threshold voltage limitation. Because the bulk-driven transistor is a depletion type device, it can work under negative, zero, or even slightly positive biasing condition.

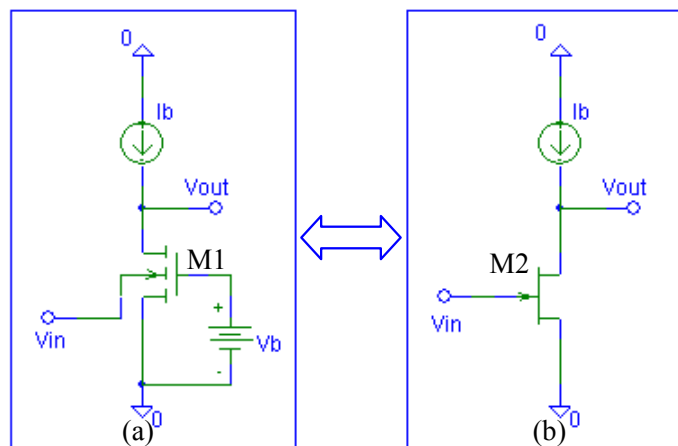


Fig. 1: Bulk-Driven MOS Transistor (a), and its equivalent JFET (b)

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To obtain a high output impedance in CMOS, a cascode stage may be placed straight on the input pair of the OTA.

The folded-cascode OTA is shown in Fig. 2. The name "folded-cascode" comes from folding down p-channel cascode active loads of a diff-pair and changing the MOSFETs to n-channels. This OTA, like all OTAs, has good PSRR compared to the two-stage op-amp since the OTA is compensated with the load capacitance.

The folded cascode input stage, as shown in figure 2. increase the common-mode input voltage range, since we replace a current source M_7 - M_8 instead of a current mirror which its used typically in the conventional OTA.

The input stages consist of a N-channel bulk driven differential pair M_1 - M_2 , folded cascodes M_9 - M_{10} , providing a level shift function, and a bulk driven current mirror M_{11} - M_{12} , providing a differential to single ended convention. The transistors M_7 - M_8 function as bias current source. In order to maximize the output current of the input stage, these current sources are biased at the same value as the tail current source of M_3 - M_4 .

Since the output resistance is one of the most important performance parameters for a current mirror, and the value of this resistance is almost equal for both gate-driven and bulk driven current mirrors, that's way it was used the bulk driven folded cascode current M_3 - M_4 biased by M_5 - M_6 , this type of connection is suitable for low voltage applications.

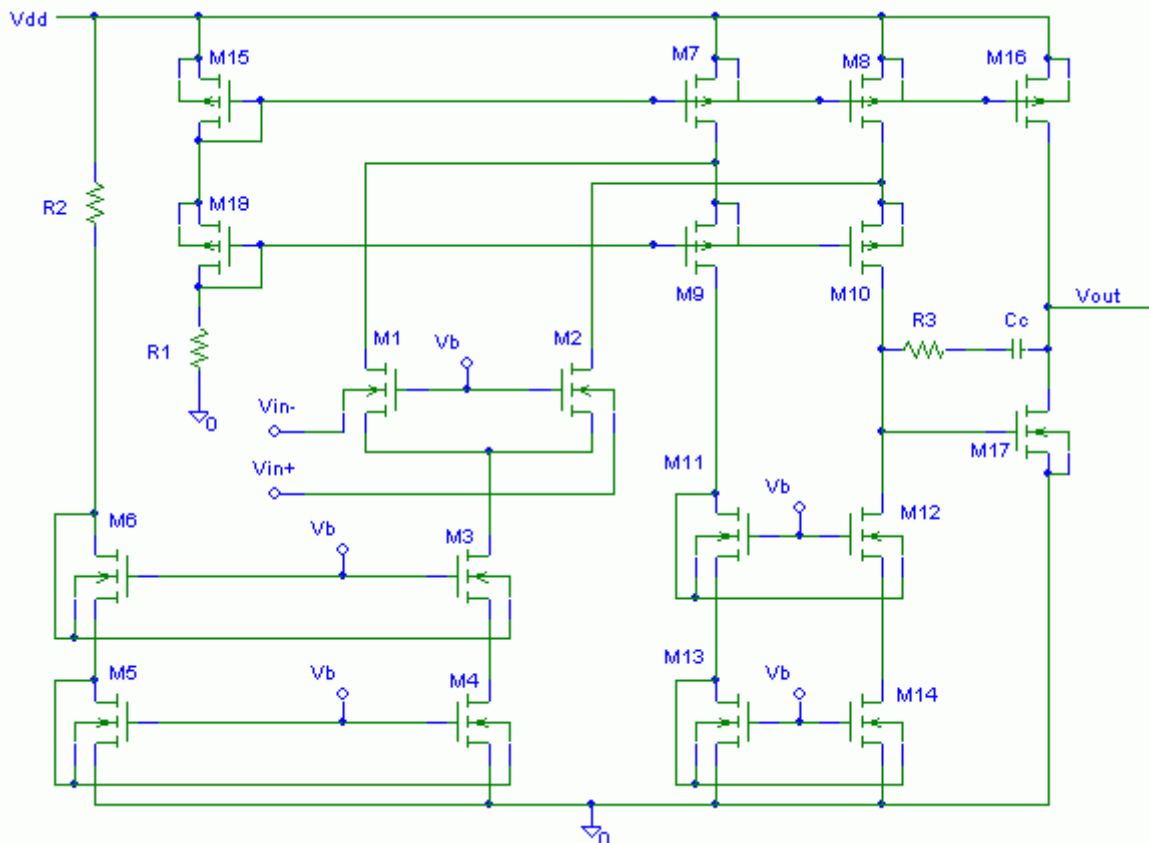


Fig. 2: *Folded-cascode Twin tub bulk-driven OTA*

The drain voltage of both input transistor can reach the positive supply voltage within one saturation voltage of the current source M_7 - M_8 . This saturation voltage is, generally, much smaller than a gate source voltage.

To simulate the folded cascode OTA it has been used the following design, since it available the N-well technology to realize it. So the technological steps and silicon area utilization needed for the Bulk-Driven technology and conventional Gate-Driven are the same.

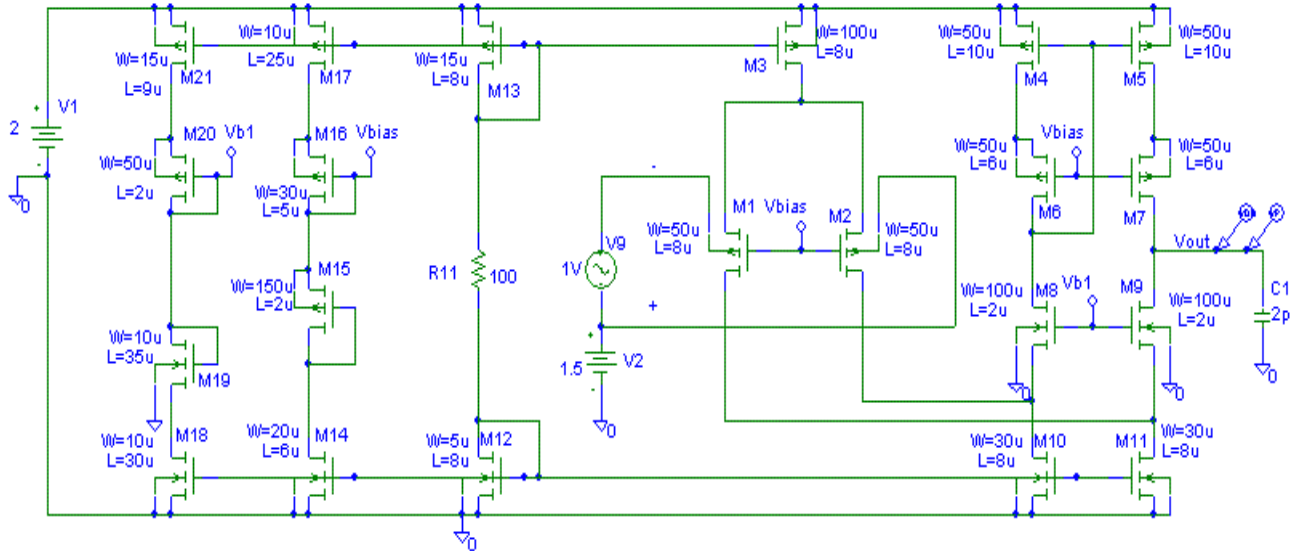


Fig. 3: *Folded-cascode N-well bulk-driven OTA*

The measurement results of the Folded-cascode N-well bulk-driven OTA are stated below:

Feature	Value	Unit
A_0	79.7	dB
Gain-bandwidth product	1.35	MHz
Offset	0.5	mV
Supply voltage	2	V
Input CMR	1.2 to 1.9	V
Slew-rate	2.6	V/ μ s
Settling time	50	nsec
Phase margin	79	Degree
Power consumption	33.7	μ W

Tab. 1: *The measurement results of the Folded-cascode N-well bulk-driven OTA*

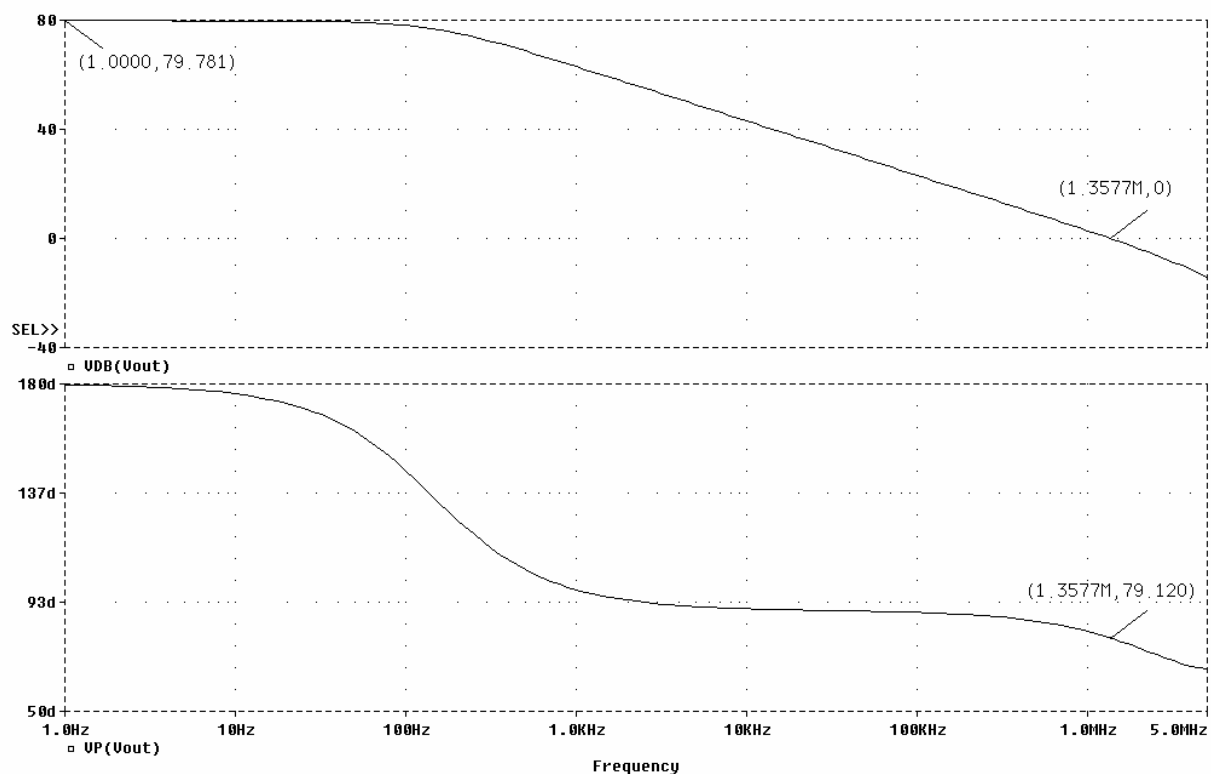


Fig. 4: *Module characteristic and Module phase characteristic of the Folded-cascode N-well bulk-driven OTA*

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REFERENCES

- [1] Satoshi, S. J, et al.: Low-Voltage CMOS Operational Amplifiers, 1995, ISBN: 0-7923-9507-7
- [2] Hogervorst, R. et al.: Design Of Low-Voltage, Low-Power Operational Amplifier Cells, 1996, ISBN: 0-7923-9781-9
- [3] Duque-Carrillo, F.: 1-V Rail-to-Rail Operational Amplifiers in Standard CMOS Technology, IEEE Journal of Solid-State Circuits, vol. 35, pp. 33 - 44, January 2000