LOW FREQUENCY IN SUBMICRON MOSFET

Ing. Martin BLÁHA, Doctoral Degree Programme (2)
Dept. of Physics, FEEC, BUT
E-mail: xblaha10@stud.feec.vutbr.cz

Supervised by: Dr. Pavel Hruška

ABSTRACT

This work discusses about Low-frequency Noise in the Metal-oxide Semiconductor (MOS) system. Is described the current-voltage and noise characteristic of an ultrahin oxide capacitor. In the concluding chapter is describe Impact of gate oxide breakdown on the noise of MOSFETs

1 INTRODUCTION

Now we work with low frequency (LF) noise (W: widht; L: lenght). The thickness of the gate oxide t_{ox} is reduced with the same scaling factor. The latter depends on the physical mechanism governing is the current fluctuations, that is, mobility fluctuations, symbolized by $\Delta\mu$ or carrier number fluctuations (ΔN). The final factor is for small-area transistor is the LF noise. For a large area transistor a 1/f noise spectrum is typically found below 10 KHz or so, one often observes so-called random telegraph signals in small devices, giving rise a Lorentzian type of spectrum.

More importantly, CMOS scaling has opened the door for radio frequency and microwave applications where is LF noise strong impact. The phase of noise voltage controlled oscillators (VCO). By other analog circuits is the low noise critical for proper device operation. It was demonstrated that the noise in very sensitive technological factors.

The figure 1 shows a roadmap for the 1/f noise spectral density (S_{VG}) of a RF transistor. The S_{VG} figure is normalized to an active device area of $1\mu m^2$.

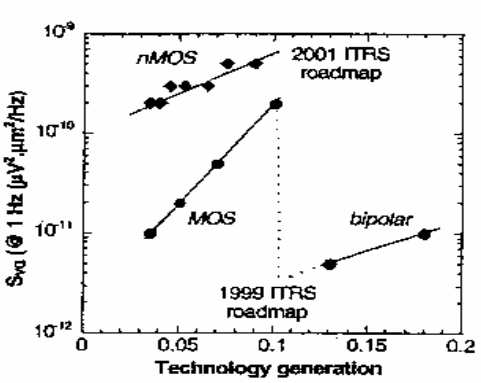

Fig. 1: *ITRS roadmap for the 1/f noise spectral density SV gate of a RF transistor. Note that SV gate is normalized to an active device area of 1 μm2 and that SV gate ~ (W.L)-1. The 1999 roadmap assumes a bipolar device through 110 nm and a MOS device for later generations. The effective gate bias, however, is not mentioned.*

When we reduction t_{ox} next increase tunneling currents. Next capture deals impact of geometrical device scaling on the noise, with emphasis on the L and t_{ox} dependence. Next to meet new materials and device architectures implemented or developed. In the fifth section as will shown switching bias operation of a transistor may reduce considerably the 1/f noise. The impact of hot-carrier degradation on the 1/f noise will be discussed.

2 LOW-FREQUENCY NOISE IN THE MOS SYSTEM

It is well estabilished that the tunneling current I_t flowing through the oxide of a MOS capacitor can exhibit 1/f noise, whereby the current spectral density S_I is proportional to I^2_t. When we applied high current then increase LF noise. Or the dielectrics go break down and behaves like a resistor.

3 CURRENT-VOLTAGE CHARACTERISTICS OF AN ULTRAHIN OXIDE CAPACITOR

There is Fowler-Nordheim tuneling throuhgt a tringular potential barrier. The current through a thin oxide capacitor is dictated by direct tunneling through a trapezoid barrier. By high – field tunel injection of the electrons into the oxide layer and the microscopic defects are generated in the Si-SiO_2 system.

Figure 2 show enrgy band diagram by Silc and soft BD.

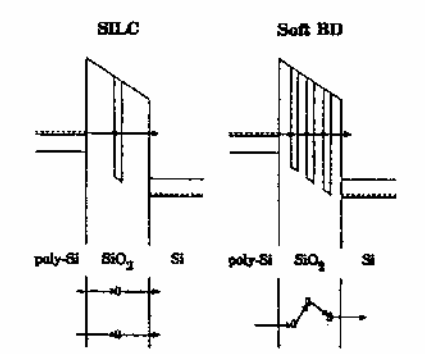

Fig. 2: *Energy band diagram of the MOS structure with the trap assisted tunneling process for the SILC and the soft breakdown phenomenon.*

4 NOISE CHARACTERISTICS OF AN ULTRAHIN OXIDE CAPACITOR

The 1/f noise was firsty pointed by ALERT. The two-levels fluctuations and more complex was observed by MOSFET system. The figure 3 shows theory where allows electron tunneling. This is call as TAT current. The corresponding RTS amplitude in the gate current ΔI_G can be expressed as

$$\frac{\Delta I_G}{I_G} = \frac{g_G}{I_G}\frac{q}{C_{ox}A_G} \tag{1}$$

In Eq. 1 is g_G the conductance of the MOS capacitor, that is, dI_G/dV_G, C_{ox} is the oxide capacitance per cm^2 and A_G is the effective area of the conductive region.

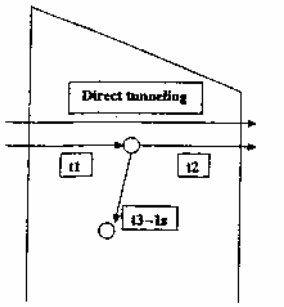

Fig. 3: *Noise generation mechanism for trap-assisted tunneling current. Time t3 is slow relaxation for the trap that gives rise to fluctuations in the tunneling times t1-t2. The time t3 is much larger than the tunneling times t1 and t2*

5 IMPACT OF GATE OXIDE BREAKDOWN ON THE NOISE OF MOSFETS

Influence is direct or indirect. First fluctuations in the gate current directly cause noise at the gate electrode.

The direct impact of the gate noise on the drain current noise has been experimentally verified, for a F-N stressed nMOSFET. Te figure 4 shows resulting of evolution of S_{ID} by the

3.3 nm gate oxide. One can see that also the drain current noise in the soft breakdown (SBD) regime becomes highly unstable and exhibits Lorentzians associated with telegraphic fluctuations. The channel noise after hard breakdown (HBD) is again predominantly 1/f like, but with orders of magnitude larger magnitude. By analyzing the gate, substrate, source, and drain current as a function of the F-N stress time, it is possible to distinguish whether the SBD or HBD percolation path in the gate oxide is closer to the source or drain or midchannel. It has been observed that for a SBD event close to the drain, the RTSs of gate an drain currents are correlated, whereas this is not the case for a SBD close to the source.[1]

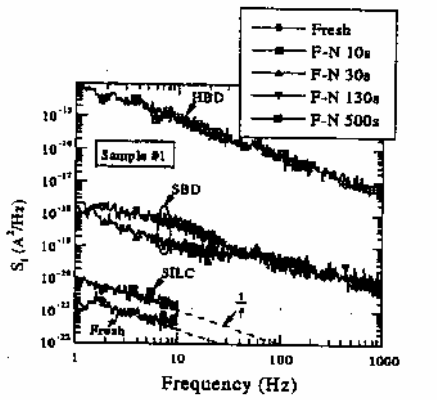

Fig. 4: *Measured drain current noise spectra (SID) with VDS=0,1V and VGS=1V for several F-N stress times*

6 CONCLUSSION

The revolution takes place in the basic structure of advanced silicon MOSFETs. For analog applications (graded-chanenel structure) is possible the novel materials and high-mobility substrates (strained silicon, germanium), the new device architectures are being explored to enhance the device performance.

REFERENCES

[1] Simoen, E., Claeys, C.: Low-Frequency Noise Performance of Scaled Deep Submicron Metal-Oxide-Semiconductor Devices

[2] Simoen, E., Mercha, A., Claeys, C., Lukyanchikova, N., Garbar, N.: Impact of the back/gate bias on the low-frequency noise of fully depleted silicon-on-insulator MOSFETs