MOS CAPACITORS

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ABSTRACT

For economical reason, it is highly desirable to implement the analog part of mainly digital system on chip in standard CMOS process. The advantages are low cost and area requirements, the disadvantages are non-linear C-V characteristics and problems resulting from it. This paper describes possibilities of using standard MOSFET gate structure as capacitor.

1 INTRODUCTION

Most analog applications require capacitors with high specific capacitance per unit area and with high linearity. These capacitors are primarily realized with a high capacitance process option, but these extra layers require additional process steps that increase the fabrication costs. One promising way how to avoid the need for nonstandard process is to implement linear capacitors using the MOSFET gate structure, which is the intrinsic element of any MOS technology. The main disadvantage of such gate capacitors is their large voltage dependence caused by different charge distributions in the accumulation, depletion and inversion region.

2 GATE STRUCTURE

Fig. 1 shows a cross section of typical gate structure and connection used as capacitor. This structure is named as MOSCAP. It is possible these structure model as serial combination of linear oxide capacitance and strong non-linear capacitance with dependence of voltage.

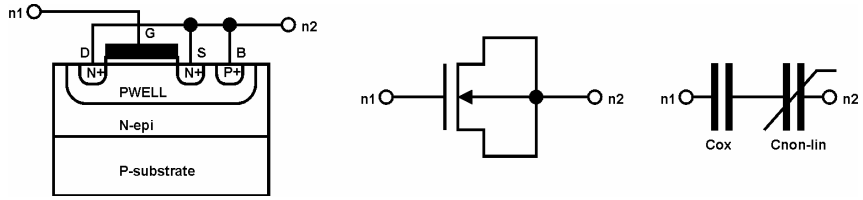

Fig. 1: *Structure of n-channel MOS transistor, connection as MOSCAP and serial model*

The C/V behavior of such a MOSCAP shows strong voltage dependence, Fig. 2. This is caused by different way of charging the device. There are three regions of this characteristic: Accumulation, Depletion and Inversion. In next section are used simplified equals to illustration of principle.

Accumulation occurs when one applies a voltage, which is less than the flat-band voltage. The negative charge on the gate attracts holes from the substrate to the oxide-semiconductor interface. Only a small amount of band bending is needed to build up the accumulation charge so that almost all of the potential variation is within the oxide. In accumulation there is no depletion layer. The remaining capacitor is the oxide capacitance, so that the capacitance equals:

$$C_{LF} = C_{HF} = C_{OX} \tag{1}$$

It is simplified equal which is valid for $V_G \leq V_{FB}$. In accumulation region capacitance for low and high frequency is the same.

As a more positive voltage than the flat-band voltage is applied, a negative charge builds up in the semiconductor. Initially this charge is due to the depletion of the semiconductor starting from the oxide-semiconductor interface. The depletion layer width further increases with increasing gate voltage. In depletion the MOS capacitance is obtained from the series connection of the oxide capacitance and the capacitance of the depletion layer and resulting capacity is smaller as both components. Result is given by:

$$C_{LF} = C_{HF} = \frac{1}{\frac{1}{C_{OX}} + \frac{x_d}{\varepsilon_S}} \tag{2}$$

where x_d is the variable depletion layer width which is calculated from:

$$x_d = \sqrt{\frac{2\varepsilon_s \phi_s}{qN_a}} \tag{3}$$

As the potential across the semiconductor increases beyond twice the bulk potential, another type of negative charge emerges at the oxide-semiconductor interface: this charge is due to minority carriers, which form a so-called inversion layer. As one further increase the gate voltage, the depletion layer width barely increases further since the charge in the inversion layer increases exponentially with the surface potential. In inversion the capacitance becomes independent of the gate voltage. The low frequency capacitance equals the oxide capacitance since charge is added to and from the inversion layer in a low frequency measurement. The high frequency capacitance is obtained from the series connection of the oxide capacitance and the capacitance of the depletion layer having its maximum width. Low and high frequency capacitance are equaled by:

$$C_{LF} = C_{OX} \tag{4}$$

$$C_{HF} = \frac{1}{\frac{1}{C_{OX}} + \frac{x_{d\max}}{\varepsilon_S}} \tag{5}$$

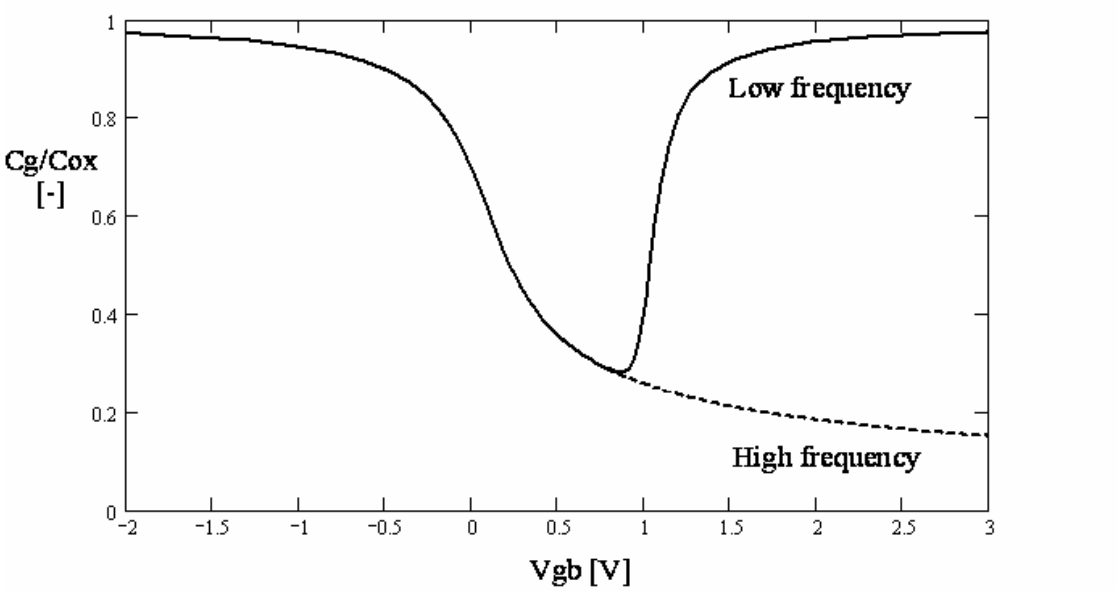

Fig. 2: *Normalized typically C-V characteristic of n-channel MOS capacitor*

3 METHODS OF COMPENZATION

It is possible to increase the width of depletion region by source-bulk bias voltage. It is shown in Fig. 3. In this area the C-V dependency is linear and it is usable for compensation techniques.

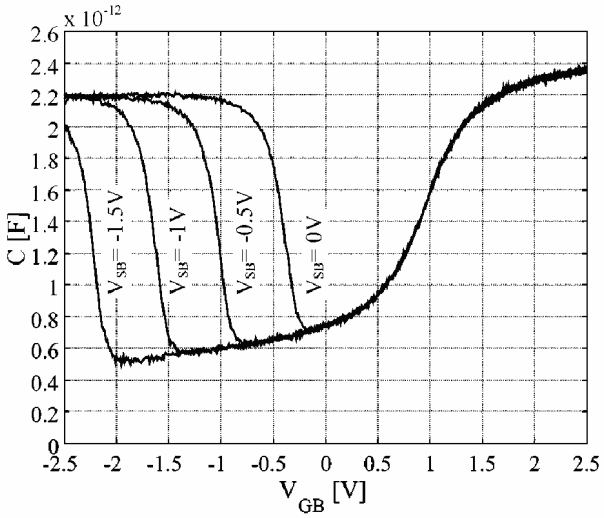

Fig. 3: *Depletion region broadening of a p-channel MOS capacitor*

3.1 SERIAL TECHNIQUE

A series nonlinearity compensation with two or more gate coupled MOS capacitors can be used to reduce this voltage dependence and provides a high-linearity capacitor. For detailed description you can see [1]. There are two MOSCAPs connected anti-serially in Fig. 4. The gate-to-bulk capacitance ones transistor in depletion is given by:

$$C_{GB} = C_{OX} \cdot \left(1 + \frac{2 \cdot \left| V_{GB} - V_{FB} \right| \cdot C_{OX}^2}{\varepsilon_0 \cdot \varepsilon_{Si} \cdot q \cdot N_B} \right)^{-1/2} \quad (6)$$

Combination of two anti-serially transistor takes total capacitance by:

$$C_{Serial} = C_{OX} \cdot \left(\sqrt{1 + \frac{2 \cdot \left| V_{GB1} + V_{FB} \right| \cdot C_{OX}^2}{\varepsilon_0 \cdot \varepsilon_{Si} \cdot q \cdot N_B}} + \sqrt{1 + \frac{2 \cdot \left| V_{GB2} - V_{FB} \right| \cdot C_{OX}^2}{\varepsilon_0 \cdot \varepsilon_{Si} \cdot q \cdot N_B}} \right)^{-1} \quad (7)$$

This compensation combines high linearity with moderate area efficiency. To prevent a gate charging in consequence of charge accumulation at node between MOSFET gates, its need connect high-resistance element on this node. It is possible to use an n-channel MOSFET on this place. This transistor is operated in the sub threshold regime. Its influence on the capacitance behavior is negligible. Its area shall be small compared to active transistors.

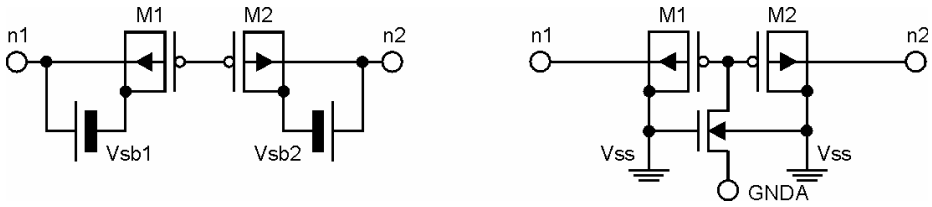

Fig. 4: *Principe and realization of serial compensation*

3.2 PARALLEL TECHNIQUE

Fig. 5 shows combination of anti-parallel transistors. Technique is described in [3]. The parallel compensation provides moderate linearity at high area efficiency. Moderate linearity is obtained for low bias voltages, but at high voltages a relatively large nonlinearity is found. Therefore, parallel-compensated depletion-mode MOSCAPs should only be used when high linearity is not required.

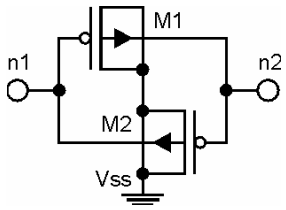

Fig. 5: *Realization of parallel compensation*

4 EXPERIMENTAL CAPACITANCE MEASUREMENTS

There are several methods how to measure the MOS capacitance.

The first method is based on impedance measurements by RLC meter. This method is simple, fast with good resolution. The maximal frequency used for measurement is above 10 MHz and accuracy is in units of fF.

The second way represents S-parameter measurements by RF signal up to GHz band. It is converting to Y-parameters and from these are calculated needy parameters like Cgs, Cgd

and Cgb. This method is slow with poor resolution, accuracy above tens of fF. A special test structure on chip surface is needed for the measurements. To eliminate parasitic capacitance of leads a calibration technique with short and open circuit should be used.

The last method is charge-based capacitance measurement. It has sub-fF resolution through on-wafer conversion of capacitance to DC current. The principle consists in driving the device under test by constantly ramped voltage and measuring capacitive current. Capacity is than equal:

$$C = \frac{I_{measure}}{dV / dt} \qquad (8)$$

5 CONCLUSION

This paper deals with problems of using of non-linear capacitors in linear systems on chip. The work presented is a part of project for design of a new type of ∑Δ modulator.

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