PASSIVE QUENCHING CIRCUIT FOR SP-QKD

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ABSTRACT

Single photons quantum key distribution (SP-QKD), more popularly known as optical quantum cryptography, uses a single-photon communications to distribute the secret keys required for secure communications. This paper describes a design of an optical receiver that is suitable for the SP-QKD. A receiver with an avalanche photodiode and a gated passive quenching circuit are presented.

1 INTRODUCTION

The quantum cryptography has been developed to securely deliver a cryptographic key. Quantum mechanical properties of single photons can be exploited to provide a secure key distribution. Alice (sender) and Bob (recipient) have a quantum channel and a conventional channel for communications between them. The quantum channel is an optical fiber or a free space. The SP-QKD uses protocol BB84 [1].

For the SP-QKD we have to able detected a single photon. Such as receivers are used avalanche photodiodes with quenching circuits. Basic requirements on the receiver are high sensitivity, low dark count rates and ability to gate for very small time (about 10 ns).

2 GATED PASSIVE-QUENCHING CIRCUITS

A Passive-Quenching Circuit (PQC) is simple circuit illustrated in Fig. 1. [3] An avalanche current is quenched itself by increasing a voltage drop on a high impedance load R_L . The APD is reverse biased trough a high ballast resistor R_L of 220K Ω . A resistor R_S senses avalanche current and voltage drop on resistor R_S is evaluated by a comparator.



Fig. 1: Passive-Quenching Circuit

In figure 2 is shown a quenching circuit that is suitable such as receiver for the SP-QKD.



Fig. 2: Gated passive quenching circuit for SP-QKD

A clock signal *Clk* (e.g. 1 MHz) is connected on a D input flip-flop circuit *IC2*. A rise time of *Clk* set a flip-flop's output to logical H a through a driver *D*, a resistor R_G and a capacitor C_G is increased voltage on the avalanche photodiode above a breakdown voltage. The Quenching circuit is activated and is able detect the photons. After a short delay (~10 ns) that is determined by an *IC1*, is set a reset input of the *IC2* to logical H. The output D of the

IC2 is set to logical L and voltage on the avalanche photodiode is reduced below the breakdown voltage.

The Avalanche photodiode is able detect photons only short time that is determined by the IC1. If a photon is detected, on the comparator's output is a short impulse that set an output IC3 to logical H. Logical H on this output determines that a photon was detected. A fall time of the *Clk* signal resets the *IC3* output to logical L and the quenching circuit is ready for a next count cycle.

Simulated waveforms of the quenching circuit are shown in a figure 3 and a figure 4. On the figure 3 are shown voltages on photodiode and resistor R_S without photon detection.



Fig. 3: Simulated pulse waveforms of a APD without photon detection

A maximal voltage drop on the resistor R_S is 42 mV. A comparator level has to set above this voltage level. The figure 4 shows voltages with detection a photon. The maximal voltage drop on the resistor R_S is 105 mV. In this case an optimal comparator reference is about 80 mV. A comparator's output will be activated only when a photon will be detected. A time delay between rise time of the *Clk* signal and achieving useful voltage on the APD is about 4 ns. This delay we will include in design of the SP-QKD transceiver.

The block diagram (fig. 2) is designed with reference to available components. As flipflop circuits are used ON Semiconductor ECLinPS Plus family MC100EP29, a delay is realised by a MC100EP195 and as a driver is used an ECL/TTL converter MC100EPT23.



Fig. 4: Simulated pulse waveforms of a APD without photon detection

3 CONCLUSIONS

The SP-QKD is new development that promises high security for high-value data. The receiver with the avalanche photodiode and the gated passive-quenching circuit is able to realize requirements that are need for correct function the SP-QKD.

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