LOW-PASS FILTER WITH UCCS BASED ON PASSIVE LADDER STRUCTURE

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ABSTRACT

This paper describes a design of a new active filter derived from an RLC ladder filter. Its basic building blocks (integrators and differentiators) are realized by universal current conveyors. The device provides high bandwidth, which confirmed PSpice simulation.

1 INTRODUCTION

Many active filter topologies are derived from the passive RLC ladder structure [1], [2]. These filters retain the convenient low sensitivities of passive ladder networks, remove bulky coils and with well-selected active devices, they have also good frequency parameters.

I will present a design of a third-order low-pass filter with universal current conveyors (UCCs) which simulates a passive-ladder structure.

2 FILTER SYNTHESIS VIA RLC NETWORK

The active filter synthesis will be done directly from an appropriately terminated passive ladder network. As an example for this design, the third-order passive filter with one transfer zero shown in Fig. 1 was chosen. State variables (voltages on capacitors and current through inductor) and input and output currents and voltages are marked in the schematic.

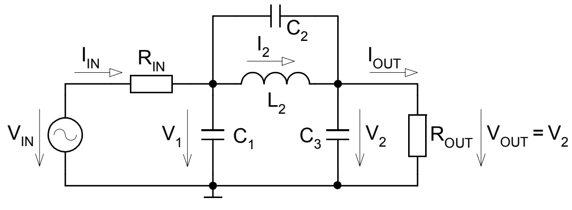


Fig. 1: *RLC prototype intended for active filter synthesis*

The synthesis is based on simulating voltage-current relations in the passive-ladder filter [1]. The following equations are valid for the network in Fig. 1.

$$I_{IN} = \frac{1}{R_{IN}}\left(V_{IN} - V_1\right), \tag{2.1}$$

$$V_1 = \frac{1}{sC_1}\left[I_{IN} - I_2 - sC_2\left(V_1 - V_2\right)\right] \;\Rightarrow\; V_1 = \frac{1}{s\left(C_1 + C_2\right)}\left[I_{IN} - I_2 + sC_2 V_2\right], \tag{2.2}$$

$$I_2 = \frac{1}{sL_2}\left(V_1 - V_2\right), \tag{2.3}$$

$$V_2 = \frac{1}{sC_3}\left[I_2 - I_{OUT} + sC_2\left(V_1 - V_2\right)\right] \;\Rightarrow\; V_2 = \frac{1}{s\left(C_2 + C_3\right)}\left[I_2 - I_{OUT} + sC_2 V_1\right], \tag{2.4}$$

$$I_{OUT} = \frac{1}{R_{OUT}} V_{OUT} = \frac{1}{R_{OUT}} V_2 . \tag{2.5}$$

Currents I_{IN} and I_{OUT} in equations (2.2) and (2.4) can be substituted by equations (2.1) and (2.5). It is necessary to convert all introduced currents to voltages for the construction of voltage-mode signal flow graph. This procedure can be done by multiplying all currents by an arbitrary resistance *R*. Thus current I_2 will be converted to new voltage V_2'. The resulting equations are:

$$V_1 = \frac{\frac{R_{IN}}{R}}{s\left(C_1 + C_2\right)R_{IN} + 1}\left(-V_2' + sC_2 R V_2 + \frac{R}{R_{IN}} V_{IN}\right), \tag{2.6}$$

$$V_2' = \frac{R}{sL_2}\left(V_1 - V_2\right), \tag{2.7}$$

$$V_2 = \frac{\frac{R_{OUT}}{R}}{s\left(C_2 + C_3\right)R_{OUT} + 1}\left(V_2' + sC_2 R V_1\right). \tag{2.8}$$

According to these equations, the block diagram shown in Fig. 2 can be drawn. It consists of damped integrators, ideal integrator, differentiators, voltage amplifier and summers. The design can also be modified in order to get only integrators in the structure [3].

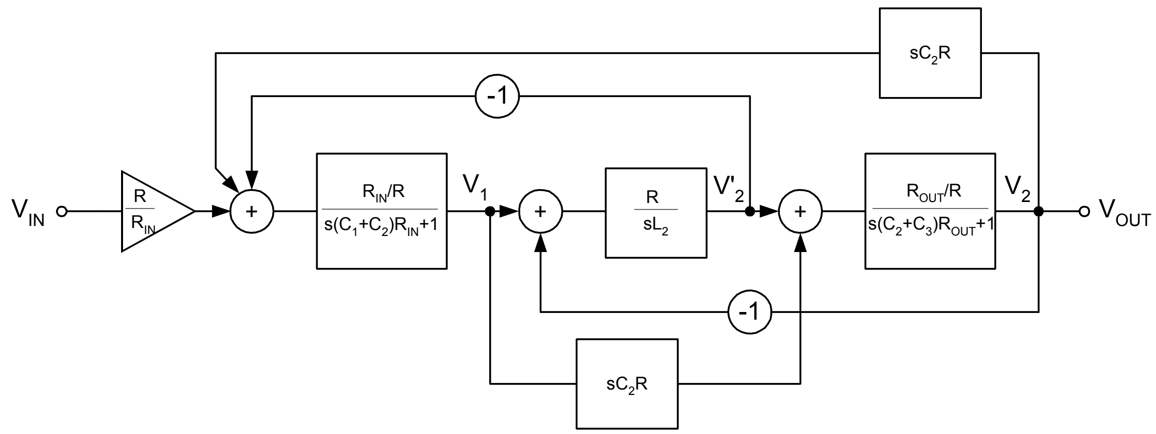


Fig. 2: *Block diagram of the low-pass passive filter shown in Fig. 1*

3 UNIVERSAL CURRENT CONVEYOR

UCC is a very versatile recently introduced active element [4]. The UCC symbol and terminal definitions are shown in Fig. 3.

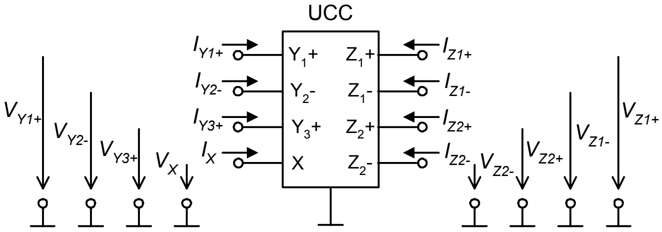


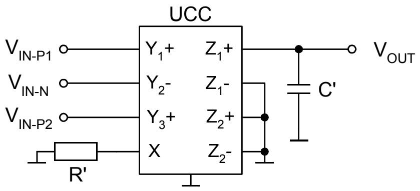
Fig. 3: *UCC symbol and terminal definitions*

The definition equations of terminal parameters are $I_{\mathrm{Y1+}} = I_{\mathrm{Y2-}} = I_{\mathrm{Y3+}} = 0$, $V_{\mathrm{X}} = V_{\mathrm{Y1+}} - V_{\mathrm{Y2-}} + V_{\mathrm{Y3+}}$ and $I_{\mathrm{Z1+}} = -I_{\mathrm{Z1-}} = I_{\mathrm{Z2+}} = -I_{\mathrm{Z2-}} = I_{\mathrm{X}}$, where I_{X} is an independent current. Multiple input and output terminals make the UCC an advantageous element for the design of active circuits with multiple feedbacks. Differential voltage inputs Y can be used as circuit inputs with high impedance or to connect multiple voltage feedbacks.

A new advanced internal structure of UCC was designed in our workplace [5]. It consists of transconductance amplifiers and should have nearly ideal parameters when specific transconductances are matched. The most critical parameters of UCC are the X-port impedance (ideally zero) and transfer bandwidths. Voltage and current frequency response has 85 MHz bandwidth for up to 10 pF capacitive load. The impedance of port X is very small up to high frequencies. The Z_{X} module is 2.7 Ω at 1 MHz and 17 Ω at 10 MHz.

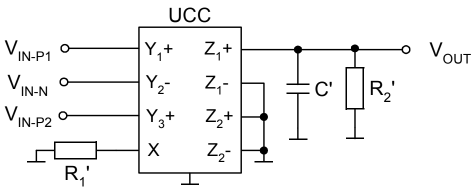
4 ACTIVE FILTER BUILDING BLOCKS

Voltage mode integrator, damped integrator and differentiator employing UCC will be introduced in this chapter. The blocks and relations for their output voltages are shown in Figs. 4, 5, 6. They have multiple inputs which will be used for voltage summation or subtraction (see Fig. 2).



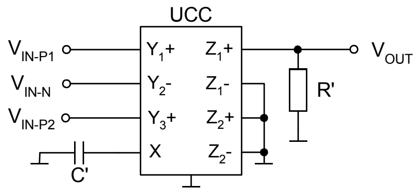
$$V_{OUT} = \frac{1}{sR'C'}\left(V_{IN-P1} - V_{IN-N} + V_{IN-P2}\right)$$

Fig. 4: *Ideal integrator with UCC and its output voltage*



$$V_{OUT} = \frac{\dfrac{R_2'}{R_1'}}{sR_2'C' + 1}\left(V_{IN-P1} - V_{IN-N} + V_{IN-P2}\right)$$

Fig. 5: *Damped integrator with UCC and its output voltage*



$$V_{OUT} = sR'C'\left(V_{IN-P1} - V_{IN-N} + V_{IN-P2}\right)$$

Fig. 6: *Ideal differentiator with UCC and its output voltage*

5 IMPLEMENTATION WITH UCCS

By implementing the described building blocks into the diagram in Fig. 2, we get the structure in Fig. 7. We assumed $R = R_{IN} = R_{OUT}$, thus the input voltage amplifier is omitted.

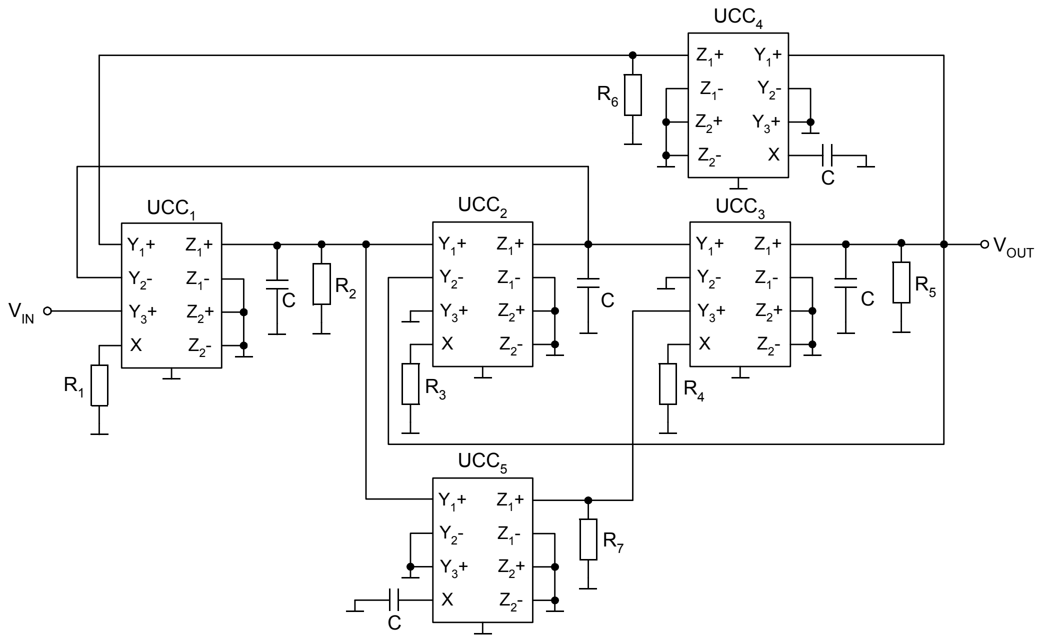


Fig. 7: *Implementation of the flow graph in Fig. 2 with UCCs*

The component parameters of active filter in Fig. 7 can be converted from the parameters of passive filter in Fig. 1 by the relations in the second row of Tab. 1. They were derived by comparing transfers of the blocks in Fig. 2 and in Figs. 4, 5 and 6. It is supposed that all capacitances in Fig. 7 have the same value *C* which should be appropriately chosen.

Tab. 1: *Relations between component parameters of filters in Figs. 7 and 1 and numerical values of resistances in Fig. 7*

Fig. 7	R_1	R_2	R_3	R_4	R_5	$R_6 = R_7$
Fig. 1	$\frac{C_1 + C_2}{C} R$	$\frac{C_1 + C_2}{C} R_{IN}$	$\frac{L_2}{RC}$	$\frac{C_2 + C_3}{C} R$	$\frac{C_2 + C_3}{C} R_{OUT}$	$\frac{C_2}{C} R$
Numerical values	3229 Ω	3229 Ω	1550 Ω	3229 Ω	3229 Ω	48.84 Ω

Numeric component parameters calculated from a passive RLC filter, which was designed by tables, are in the bottom row of the Tab. 1. The filter has the Cauer approximation, 1 MHz cut-off frequency, 1 dB pass-band ripple and 60 dB minimum stop-band attenuation. The capacity C was chosen 100 pF, the resistances $R = R_{IN} = R_{OUT} = 1\ \text{k}\Omega$.

6 COMPUTER SIMULATION

The simulated frequency characteristic of the designed filter with parameters computed above is shown in Fig. 8. The PSpice model of UCC was used. It is based on the new advanced structure described in chapter 3. The characteristic is shifted 6 dB upwards, because passive ladder filters have 6 dB pass-band attenuation due to terminating resistances.

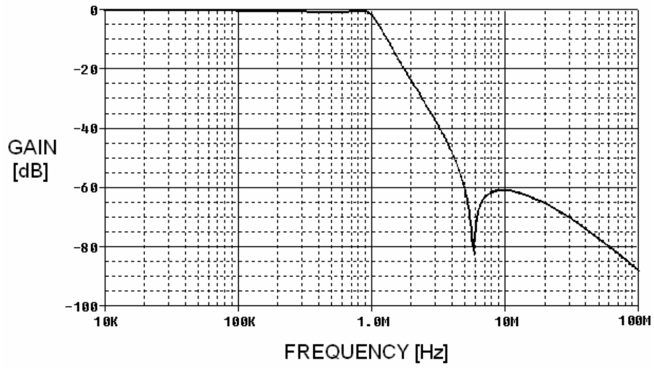


Fig. 8: *Simulated module frequency characteristic of the proposed filter*

7 CONCLUSION

A low-pass filter structure based on RLC ladder filter was designed. It consists of integrators, differentiators connected in feedback and feedforward loops. The universal current conveyor was used as a main active building block. Its new advanced internal structure allows high-frequency signal processing. PSpice simulation verified the correct function of the proposed filter with relatively high-frequency signals.

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